High-Temperature Reliability of 4H-SiC Vertical-Channel Junction Field-Effect Transistors (VJFETs) for Power Conditioning System Applications

L. Cheng [1], P. Martin [2], M. S. Mazzola [1, 2], V. Bondarenko [2], H. Causey [2], J. R. B. Casady [1], and J. B. Casady [1]

[1] SemiSouth Laboratories, Inc.
201 Research Blvd., Starkville, MS, 39759 (USA)
Phone: 1-662-324-7607, Fax: 1-662-324-7997
Email: lin.cheng@semisouth.com, Web-site: www.semisouth.com

[2] Center for Advanced Vehicular Systems (CAVS), Mississippi State University
200 Research Blvd., Starkville, MS 39759 (USA)

Abstract

Reliability of SiC devices is of critical importance in field-effect transistor (FET)-controlled devices for power conditioning system applications. In this work, we report the recent results of high-temperature reliability testing of the 600-V, 8-A, 4H-SiC Vertical-Channel Junction Field-Effect Transistors (VJFETs) fabricated in house. For studying the on-state stability, the devices were mounted on a hot-plate and thermally stressed at 275 °C in air for over 650 hours. After the 650 hours thermal storage, standard deviation of the specific on-resistance was about 0.32 at gate bias (V_{GS}) of 3 V, while the forward current reduced more at higher drain-source voltage (V_{DS}) and higher gate bias. In addition, sensitivity of the gate control on forward characteristics has also been investigated. To monitor the off-state stability of the SiC VJFET, a high temperature reverse bias (HTRB) measurement was performed under V_{GS} of -27 V and V_{DS} of 200 V at 200 °C for 2001 hours. The drain-source and gate-source reverse leakage current were reduced after the first 400 hours HTRB at 200 °C in air then remained virtually unchanged up to 2001 hours.

Key words: silicon carbide, vertical-channel, junction field-effect transistor (JFET), high-temperature, reliability, and HTRB.

1. Introduction

Among wide band-gap semiconductor-based electronics, silicon carbide (SiC)-based electronics has received an enhanced attention [1-3] for high-temperature and high-power applications such as power conditioning system that mainly related to the operation of power switch(es). However, although the remarkable results of SiC over conventional semiconductor such as silicon (Si) have been demonstrated by many groups, there is still a question on how reliable SiC can be as a material choice for commercial power devices.

Reliability of SiC devices is of critical importance in FET controlled devices such as VJFETs for power conditioning systems. Compared to bipolar junction transistor (BJT), power FET eliminates any effects from forward and reverse recovery due to its unipolar nature [4]. The inherent physical properties of SiC are well-suited for semiconductor electronic devices. Theoretical appraisals have suggested that SiC power FETs and diode rectifiers would operate over higher voltage and temperature ranges, have superior switching characteristics, as well as have die sizes nearly twenty times smaller than correspondingly rated silicon-based devices [1]. This would enable large improvements on power system performance. To demonstrate capabilities that are commonplace to well-developed silicon power components in use today, SiC power devices must: (1) block high voltages in the off-state with negligible leakage current, (2) carry high on-state currents with minimal parasitic voltage drop, (3) rapidly switch back-and-forth between on-state and off-state, (4) function reliably without a single failure over the operational lifetime of the system, and (5) be cost-effective to produce and incorporate into high power systems. In SiC, material defects in present day are the main cause of many technological challenges faced by SiC devices, which could result in:

- Higher leakage current

- Degradation of forward conduction
- Reduced critical electric field in devices
- Reliability issues

Material defects may also cause filaments that concentrate the micro-plasma of the avalanche current during reverse bias operation hence fail the devices. All of these would trade off some advantages of SiC over conventional semiconductors and may seriously hurt the reliability of the SiC power devices.

Among the SiC power devices, SiC JFET is the only controlled turn on/off SiC device that is free from gate oxidation and high-temperature metal-semiconductor Schottky barrier reliability issues. Due to the vertical-channel, SiC VJFETs enable higher packing density, lower on-resistance, and easier fabrication at reduced cost [5]. Previously, we have fabricated and demonstrated the fast switching (41 MHz), 2.5 mΩ·cm^2, 600-V 4H-SiC VJFETs with the vertical-channel structure [6]. In this work, we examined the commercial viability of the 4H-SiC VJFETs by performing a high temperature reliability testing of them.

2. Device Fabrication

A schematic of cross-sectional device structure of the 4H-SiC VJFET is shown in Figure 1. In this structure, the n-type drift, channel and source regions are epitaxially grown on an n$^+$, 8 °-off, Si-faced, 4H-SiC substrate. Trenches are then etched and implanted with Al to form p-type gates, followed by a post-implantation anneal and the formation of metal contacts. The spacing between the Al implanted region is the vertical channel region. The drain to source conduction is regulated by the channel depletion width, which is temperature-dependent and controlled by the gate bias. The source and gate Ohmic metal contacts were realized by an advanced self-aligned process.

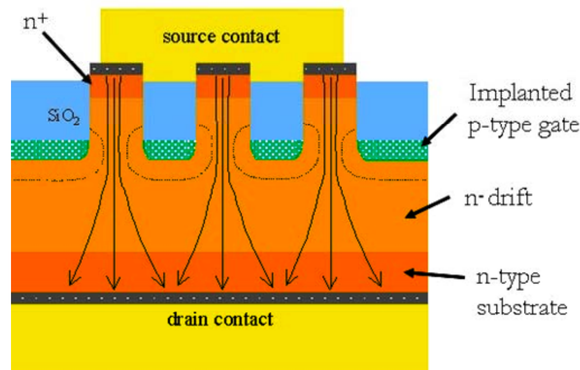

Figure 1: A schematic of cross-sectional device structure of the 4H-SiC VJFET.

3. On-state Stability Test

To study the stability of the devices in the on-state, they were mounted on a hot-plate and thermally stressed at a constant ambient temperature of 275 °C in air over time. The devices are brought to room temperature and the forward *I-V* characteristics are measured periodically. Figure 2 shows forward conduction of the VJFETs at gate bias (V_{GS}) from 0 V to 3 V before, during, and after 650 hours thermal storage. The drain current was reduced within the first 144 hours then remained virtually

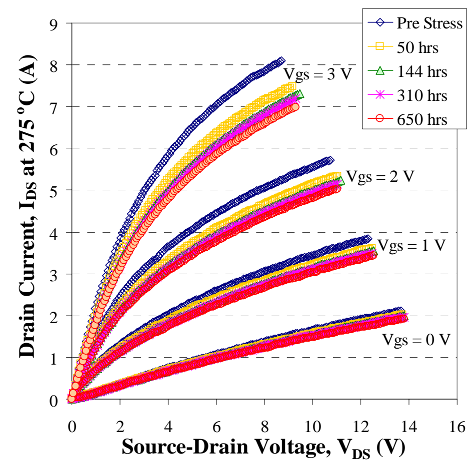

Figure 2: Forward I-V characteristics of the 4H-SiC VJFET before and after 650 hours thermal storage at 275 °C in air.

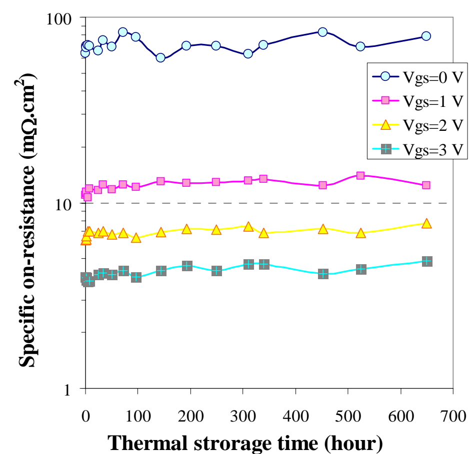

Figure 3: Specific on-resistance as a function of gate bias is measured from 0 to 650 hours of thermal storage at 275 °C in air.

unchanged for up to 650 hours. Also notice that reduction of the drain current over time was larger at higher gate bias and higher drain-source voltage, VDS. More details will be discussed next.

Figure 3 shows specific on-resistance as a function of gate bias from 0 to 650 hours of thermal storage. Standard deviation of the specific on-resistance from 0 to 650 hours of thermal storage was about 0.32 at gate bias (V_{GS}) of 3 V. It can be seen that the specific on-resistance remains relatively unchanged after the 650 hours thermal storage, which is also confirmed in Figure 4 by looking at drain current versus gate voltage at drain voltage of 0.15 V.

It is more clearly in Figure 4 that the drain current degraded more at higher drain voltage and higher gate bias. This might be due to the fact that more material defects can be involved or stimulated under higher electrical field stress at high temperature, which affect on both on-resistance and channel depletion width.

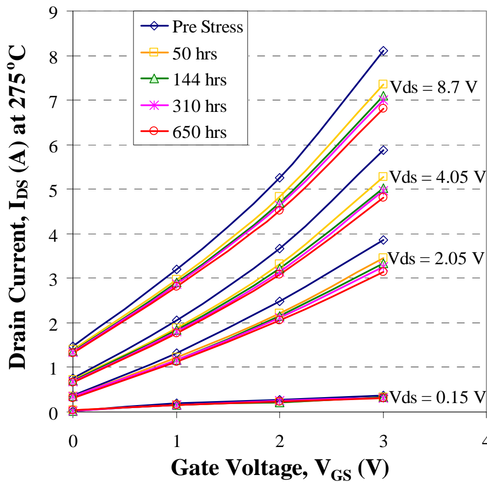

Figure 4: Drain current as function of gate bias at drain voltage of 0.15 V, 2.05 V, 4.05 V, and 8.7 V from 0 to 650 hours of thermal storage.

To examine the reliability of gate control sensitivity on forward conduction, changes in drain current at each increment of gate bias under different drain voltage (2.05 V and 8.7 V) were investigated before, during, and after 650 hours thermal storage. As shown in Figure 5, the slight change in drain current at each increment of gate bias is found to occur mostly within the first 144 hours of the thermal storage. An increment of higher gate bias results in higher degradation of drain current at higher drain voltage within the first 144 hours thermal storage. After the first 144 hours, there are no significant variations of changes in drain current at both selected drain voltages under different increment of gate bias. This indicates an excellent stability of a gate control on the forward conduction of the SiC power VJFETs.

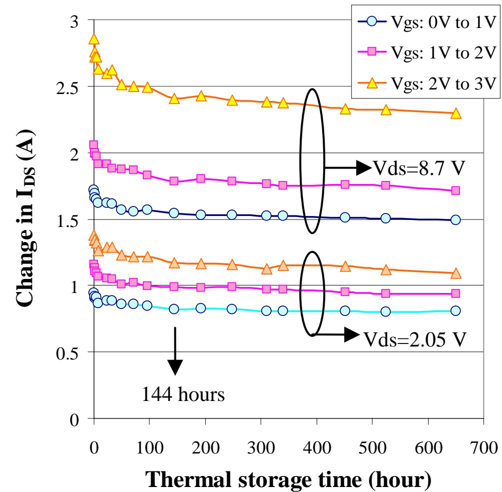

Figure 5: Change in drain current at each increment of gate bias under drain voltage of 2.05 V and 8.7 V from 0 to 650 hours of thermal storage.

4. Off-state High-Temperature Reverse Bias (HTRB) Test

4.1 Pre-stress reverse-bias characterization

High temperature reverse bias (HTRB) measurements are performed at 200 °C to monitor the

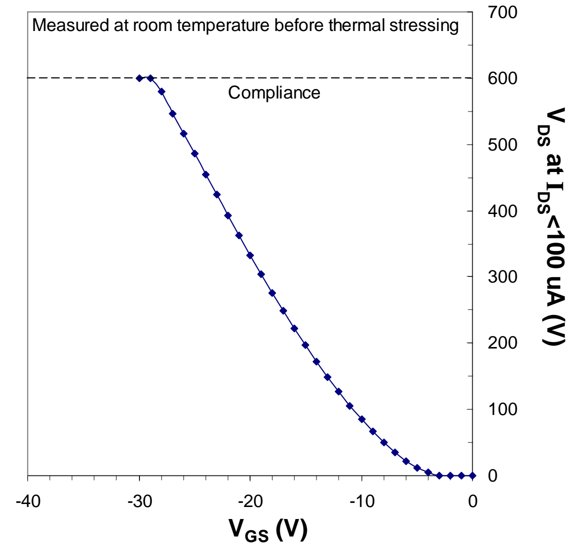

Figure 6: Drain-source reverse blocking voltage vs. gate bias of the VJFET at $I_{DS} < 50\ \mu A$ at room temperature before HTRB test.

reliability of a 600-V, 8-A VJFET during the off-state operation. Blocking characteristics of drain-source and gate-source of the VJFET before the HTRB test are shown in Figures 6 and 7, respectively.

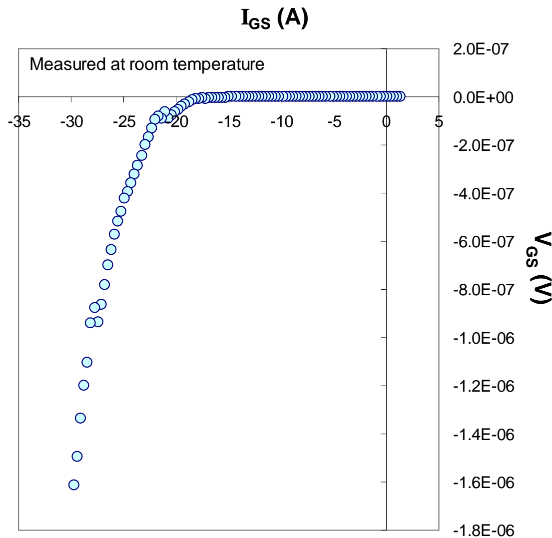

Figure 7: Reverse leakage current of gate-source of the VJFET at RT before HTRB test.

4.2 Test System Set-up

To conduct this test, an HTRB test system was designed to source operating voltages and measure the resulting currents of multiple Vertical Junction Field Effect Transistors (VJFETs) under reverse bias for long periods at high temperatures. The system capabilities include (1) reverse bias gate to source voltage from 0 to -110 Vdc, (2) drain to source voltage from 0 to 600 Vdc, (3) transistor operating temperatures up to 250 °C. A 300 °C upgrade is in process. System hardware consists of an oven to maintain the devices at high temperature, a transistor test fixture built into the oven door to facilitate easy insertion and removal of transistors, and a data acquisition rack that houses instrumentation and a computer for controlling the test system. The test system software provides the system user interface, controls the test instrumentation, and provides spreadsheet and charts for graphical data display in real time.

At the beginning of the test using Keithly Source Measurement Units (SMUs), the group gate voltage is ramped until the specified reverse bias gate voltage is obtained and then the group gate current is compared to the specified maximum group gate current. If the current is larger than the maximum group gate current, the individual gate currents are scanned and compared to their individual maximum group gate current. Transistors with excessive gate currents are eliminated from further testing. Moreover, the drain voltage for remaining transistors is ramped to the test voltage and repetitive scanning of the devices is initiated. The scan interval is the time between scans and the scan rate is the time between measuring currents for individual transistors. Both of these times are test parameters that are assigned values at the beginning of the test.

During the evaluation of each transistor, the gate and source currents are measured and the drain current is calculated using the following equation:

$$\mathbf{Ids = -(Igs+Is),}$$

as shown in the schematic diagram for the transistor under test in Figure 8. Next, gate and drain currents are compared to their corresponding maximum and minimum allowed values for the device. If the current values are not within the specified limits, the device is removed from further testing. At the end of each scan all of the current values are logged to a file. When the test is manually stopped or automatically stopped by the system, the drain voltage is first ramped to zero and then the gate voltage is ramped to zero.

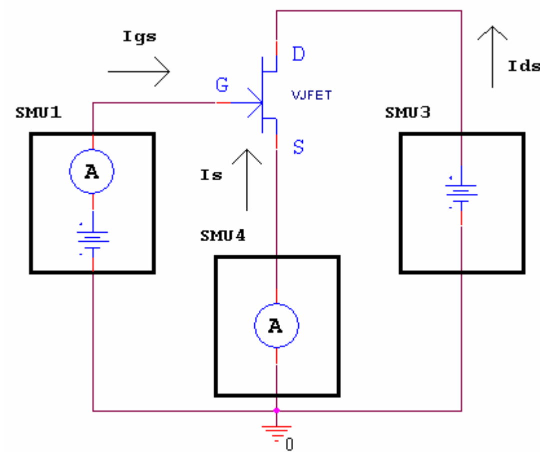

Figure 8: Schematic Diagram for Transistor Under Test (DUT)

4.3 HTRB measurement

A 600-V, 8-A SiC VJFET was packaged and exposed to air at 200 °C under a reverse drain bias of 200 V and a reverse gate bias of 27 V in an oven. A sample data up to 2001 hours is shown in Figure 9. With respect to the HTRB stress, the drain-source and the gate-source reverse leakage currents of the VJFET were negligible. It can be seen in Figure 9

that the reverse leakage currents slightly decreased within the initial 400 hours HTRB test. After the first 400 hours, the reverse leakage currents remained very reliable at 200 °C in air for up to 2001 hours. This result once again demonstrates the advantage of JFET over MOSFET by eliminating the concern on charge movement or trapping in the gate oxide of MOSFET during the long-term operation.

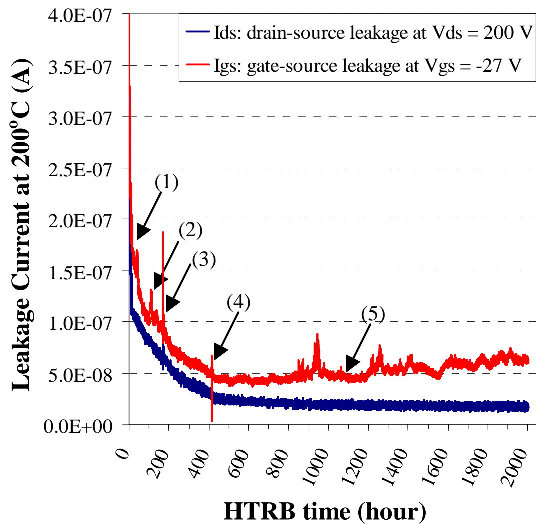

Figure 9: High Temperature Reverse Bias (HTRB) measurement showing drain-source and gate-source reverse leakage current at VDS of 200 V, VGS of 27 V and 200 °C. Because this is a new test system, the life test was interrupted at several intervals (labeled) to address technical issues.

5. Summary

High-temperature reliability testing were performed on the 600-V, 8-A, 4H-SiC Vertical-Channel Junction Field-Effect Transistors (VJFETs). Forward *I-V* characteristics of the VJFETs were studied from 0 to 650 hours of thermal storage at 275 °C in a wide-opened ambient. Off-state stability of the VJFET was investigated at 200 °C in air for 2001 hours using the HTRB technique. Preliminary results show that SemiSouth's SiC power VJFETs are reliable to operate with excellent gate control at on-state mode and very stable to operate with negligible reverse leakage currents at off-state mode. In conjunction with successful accelerated testing at 450 °C as reported in [7], these results show an early promise of commercial viability of our 4H-SiC VJFET devices.

6. Acknowledgment:

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