BAKKALAUREATSARBEIT

Switching behaviour from MOSFET gate drivers in half bridge power stages

FACHHOCHSCHULE TECHNIKUM WIEN
STUDIENGANG ELEKTRONIK/WIRTSCHAFT, 5. SEMESTER
WS 2006/2007

Andreas Hoffelner
Am Moos 47
3340 Waidhofen / Ybbs
Matr. Nr.: 0510255057

Betreuer:
Dipl.-Ing. Dr. Gerd Schauer

Wien, 20.03.2007 _____

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Abstract

In electronic devices low loss power switches are a very important part. One way to realize these switches is by using the power MOSFETs technology. In order to be able to use the full potential of these parts, a sophisticated driving concept is required. In the course of these bachelor work a self made test board with MOSFETs and monolithic gate driver circuit was developed and realized. The exemplified theory could be proved by the measurement results during switching processes in the half bridge stage. In such circuitries power losses and costs should be kept as small as possible. To follow this demand even faster switching power semiconductors were produced. The creation of a basic concept, the correct selection of the gate driver system and the technical realization from such a half bridge power stage is the topic of this work.

Kurzfassung

Verlustarme Leistungsschalter aktueller Schaltungskonzepte sind in elektronischen Baugruppen nicht mehr wegzudenken. Eine Art diese Schalter zu realisieren geschieht unter anderem mit Leistungs- MOSFETs. Um das volle Potential dieser Bauteile nutzen zu können, bedarf es an ausgefeilten Ansteuerkonzepten. Im Zuge dieser Bakkalaureatsarbeit wurde ein Testaufbau mit MOSFETs und monolithischen Treiberschaltkreisen realisiert, in welchem man die zuvor erläuterte Theorie mit Messungen während den Schaltvorgängen an den Treiberstufen und den Leistungsschaltern belegte. Man ist bestrebt die Verlustleistung und Kosten in solchen Leistungsteilen so gering wie möglich zu halten. Dieser Forderung kommt man mit immer schneller schaltenden Leistungshalbleitern nach. Die Erstellung eines Grundkonzeptes, die korrekte Auswahl des Ansteuersystems und die technische Realisierung solch einer Halbbrückenschaltung ist Thema dieser Arbeit.

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1 Introduction

This work gives a short overview at MOSFET gate drivers for switching applications. The given conceptual formulation contained the gate drive circuitry of a half bridge stage for a solar inverter, realised with power MOSFETs. The main attention was given at the practical realisation on such circuitries for power systems in the industrial electronic. For me as an technical engineer and hardware designer it is very important to understand how such systems work and what I can do to optimize it in industrial compliance, quality and cost. To discuss and writer on such subjects, it is necessary to study the basics on the main parts. This was the motivation on writing the theoretical background. A practical realisation and evaluation on the theoretical facts shows the second part of this work. This document act as a short summery for my future developments in technical engineering on MOSFET gate drivers.

2 Theoretical Background

2.1 Power MOSFET

The power MOSFET is a specific type of metal oxide semiconductor field effect transistor. It was designed to handle large power, high commutation speed and good efficiency. The MOSFET is a three terminal device where the gate source voltage controls the flow of current between the output terminals, the source and the drain. Figure 1 shows the device and figure 2 the schematic symbol. A complete detailed description on the power MOSFET could be looked up in [MUR03].

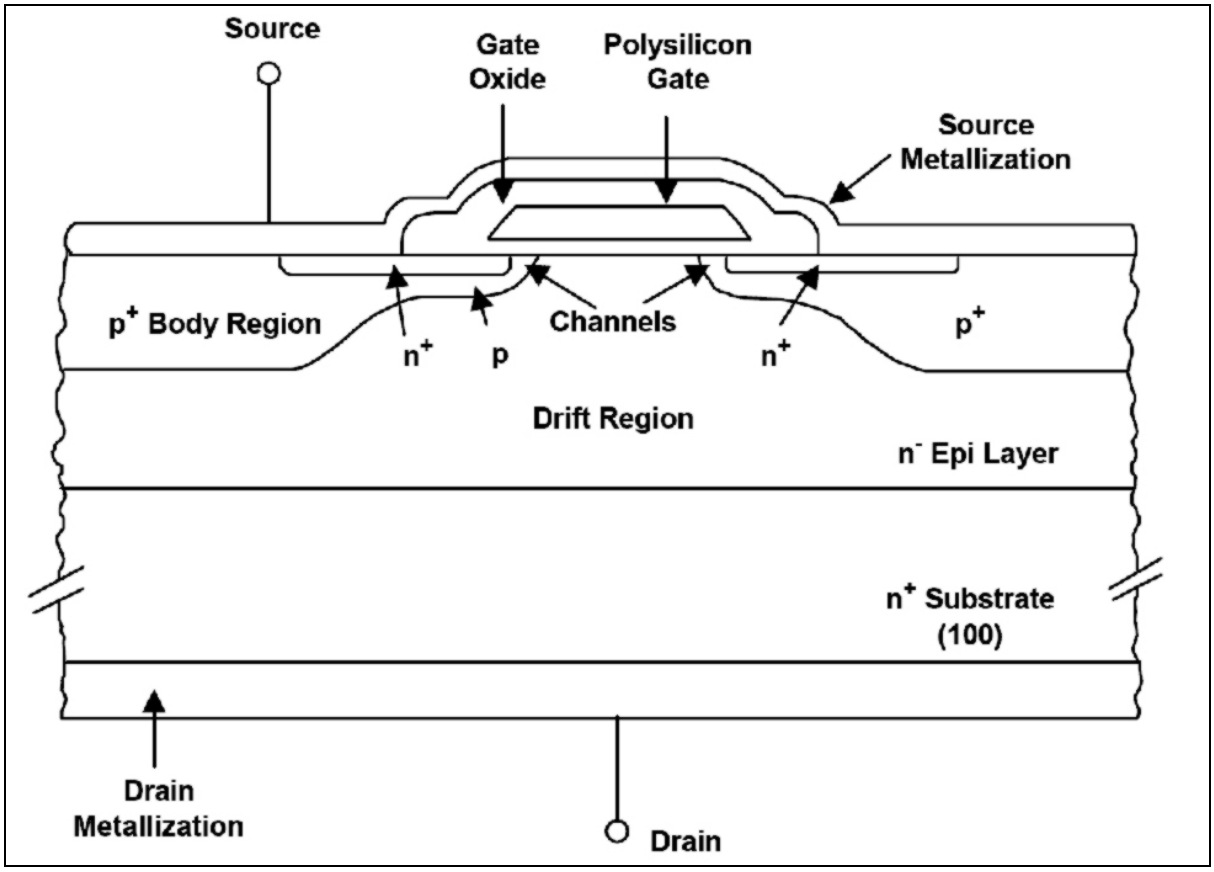


Figure 1. Vertical cross-section of an n-channel power MOSFET

The invention on the MOSFET was partly driven by the limitations of bipolar power junction transistors (BJT). The BJT is a current controlled device. A large base drive current as high as one-fifth of the collector current is required to keep the device in the on state. Also, higher reverse base drive currents are required to obtain fast turn-off. In spite of the very advanced state of manufacturability and lower costs of BJTs, these limitations have made the base drive circuit design more complicated and expensive than the power MOSFET. They are in high frequency applications better than BJTs where switching power losses are important. MOSFET are voltage controlled devices.

Because of the isolated gate electrode from the semiconductor the input impedance is very high. The required gate current during switching transient as well as the on and off states is small in contrast to the BJT.

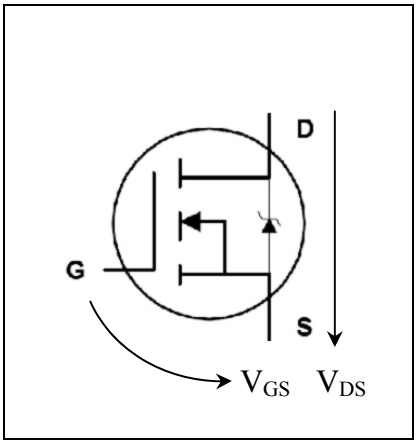


Figure 2. Schematic Symbol of an n-channel power MOSFET

MOSFETs also can easily be paralleled because the forward voltage drop increases with increasing temperature, ensuring an even distribution of current among all components. At BJTs this effect is vice versa.

2.1.1 Current Voltage Characteristics

The output characteristics for an n-channel MOSFET, drain current as a function of drain source voltage with gate source voltage as parameter are shown in figure 3. B_{VDSS} is the maximum drain to source voltage [OH00].

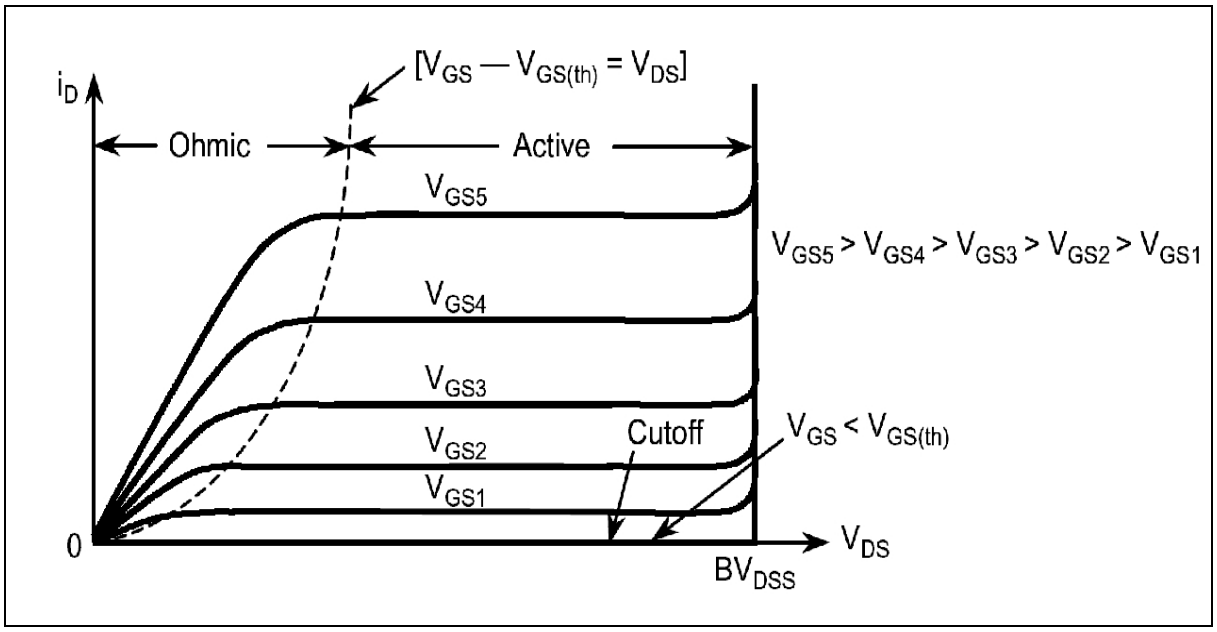


Figure 3. Output characteristics

When the device is driven by large gate source voltage, it is driven in the ohmic (constant resistance) region where the drain source voltage is small.

$$V_{GS} > V_{GS(th)}$$
$$V_{DS} < V_{GS} - V_{GS(th)}$$

In this region the power dissipation at high drain currents can be kept within save operation area by minimizing the drain source voltage. In the active (constant current, saturation) region the drain current is independent of the drain source voltage and depends only on the gate source voltage.

$$V_{GS} > V_{GS(th)}$$
$$V_{DS} > V_{GS} - V_{GS(th)}$$

In the cut off region the gate source voltage is smaller than the threshold voltage.

$$V_{GS} < V_{GS(th)}$$

The transfer curve, a plot of drain current versus gate source voltage with the MOSFET in the active region is shown in figure 4.

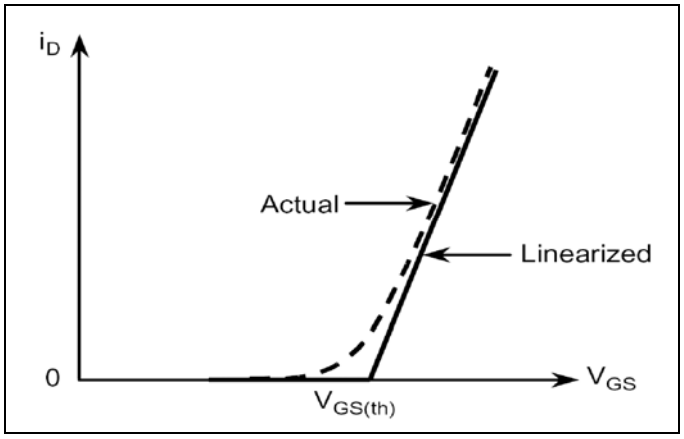


Figure 4. Transfer curve

The threshold voltage $V_{GS(th)}$ is defined as the minimum gate electrode bias required to form a conducting channel between the source and the drain.

2.1.2 Switching characteristics

The switching performance of a MOSFET is determined by the time required to establish voltage changes across capacitances. In figure 5 the circuit shows the components that have the greatest effect on switching. R_G is the distributed resistance of the gate and is approximately inversely proportional to the active area. L_S and L_D are source and drain lead induct-

ances and are around a few tens of nH. Typical values of input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances are given in the technical data sheets. The capacitances are defined in terms of the equivalent circuit capacitances as:

$$C_{iss} = C_{GS} + C_{GD},\ C_{DS} \text{ shorted}$$
$$C_{rss} = C_{GD}$$
$$C_{oss} = C_{DS} + C_{GD}$$

Gate to drain capacitance, C_{GD}, is a nonlinear function of voltage and is the most important parameter because it provides a feedback loop between the output and the input of the circuit. C_{GD} is also called the Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances. The drain source capacitance does not materially affect any of the switching characteristics or waveforms. However, it should be considered when designing a snubber circuit.

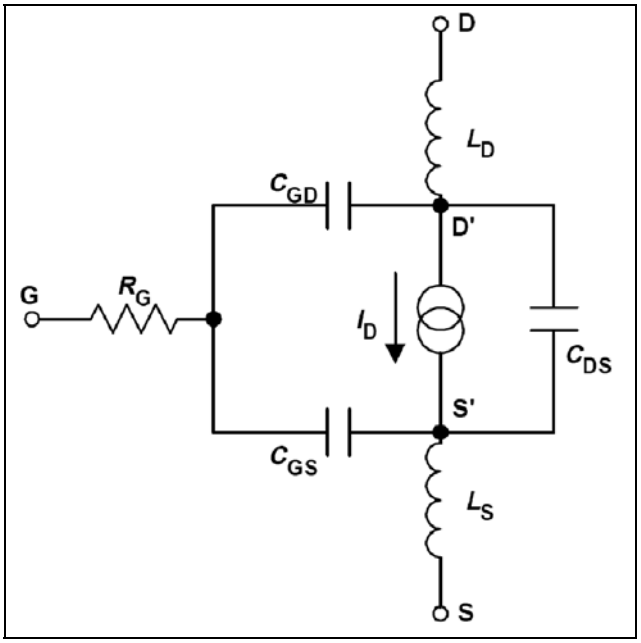


Figure 5. Equivalent MOSFET circuit

By comparing the switching performances of two devices from different manufacturers input capacitance values are useful but they do not provide accurate results. Effects of device size and transconductance (the slope of the transfer characteristic) make such comparisons more difficult. A more useful parameter from the circuit design point of view is the gate charge. Most manufacturers include both parameters on their data sheets. The following types of charges are mentioned in the datasheets.

Q_g … total gate charge (the amount of charge during $t_0 \sim t_4$ in figure 6)
Q_{gs} … gate source charge (the amount of charge during $t_0 \sim t_2$ in figure 6)
Q_{gd} … gate drain (Miller) charge (the amount of charge during $t_2 \sim t_3$ in figure 6)

The advantage of using gate charge is that the designer can easily calculate the amount of current required from the drive circuit to switch the device on in a desired length of time because of:

$$Q = C \cdot V = I \cdot t$$

For example, a device with a gate charge of 20 nC can be turned on in 20 μsec if 1 mA is supplied to the gate or it can turn on in 20 nsec if the gate current is increased to 1 A. These simple calculations would not have been possible with input capacitance values.

2.1.3 Switching waveforms

To switch a MOSFET in the on state the only charges that must be moved are the gate source and gate drain capacitance [OH00]. A typical gate charge test circuit with a diode clamped inductive load helps us to explain these effects on this event.

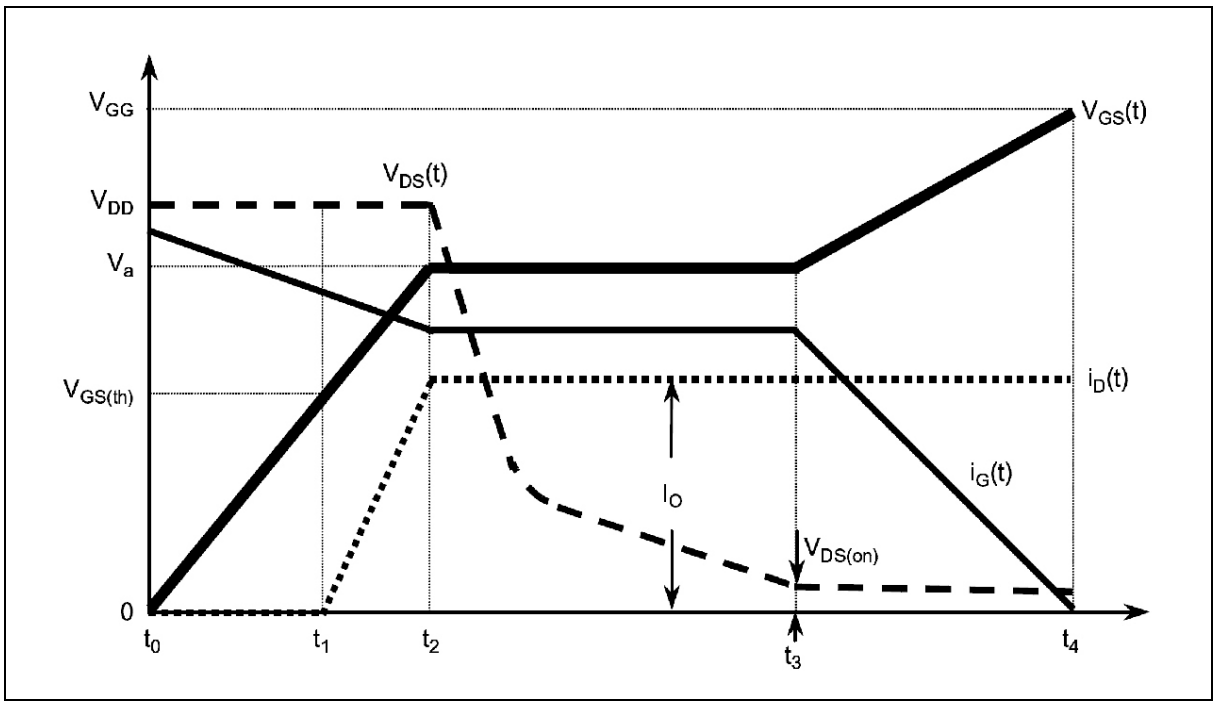


Figure 6. The Graph of $V_{GS}(t)$, $i_G(t)$, $V_{DS}(t)$, $i_D(t)$ when the MOSFET is turned on

The inductive load is modeled as a constant current source I_0 in parallel with a ideal free wheeling diode D_F with a zero reverse recovery current. The gate is driven by an ideal voltage source V_{GG} in series with the external gate resister R_G. Figure 6 shows the gate source voltage, gate source current, drain source voltage, and drain source current during turn on. They are divided into four sections (t_1, t_2, t_3 and t_4). At t_0 V_{GG} is applied to the circuit.

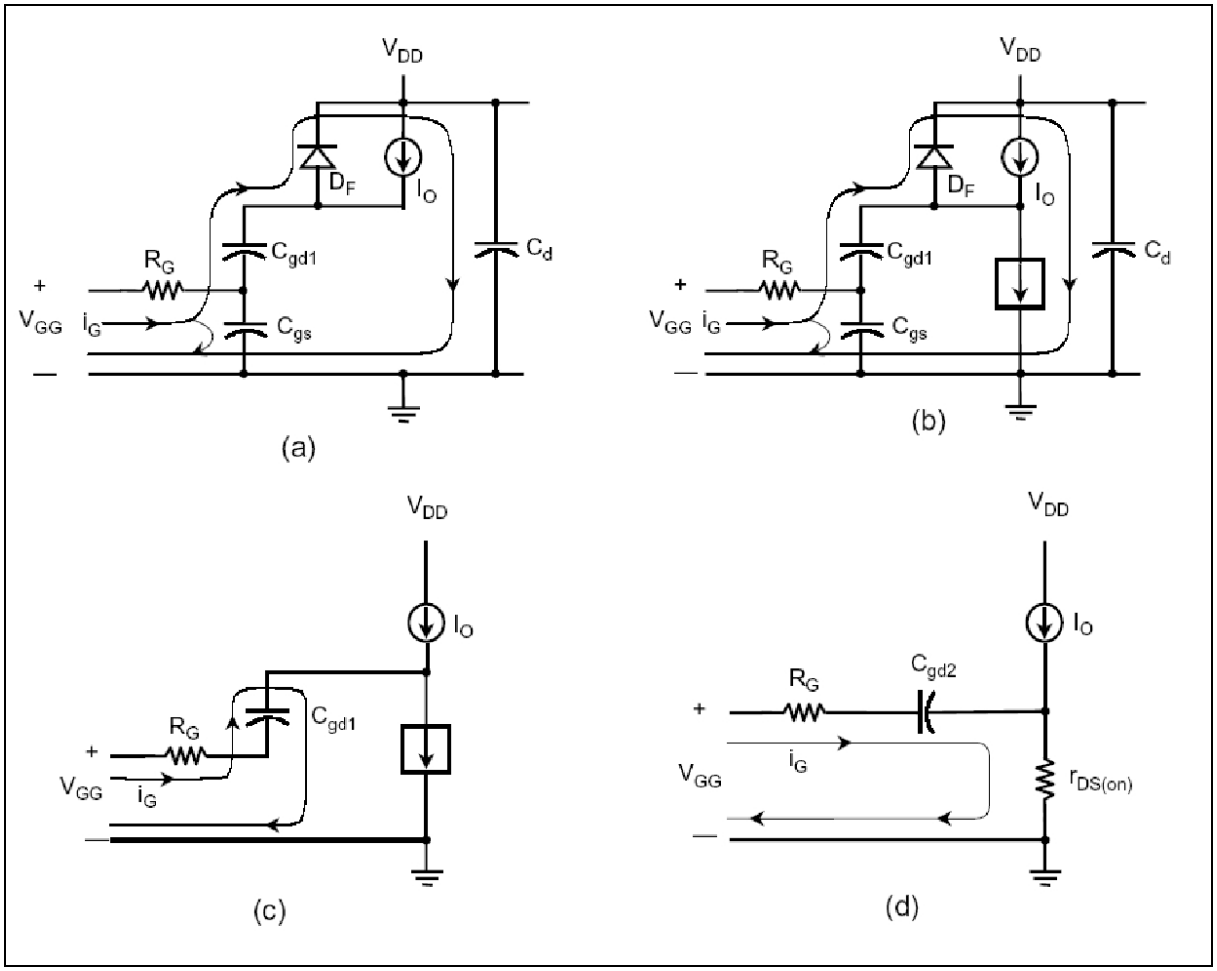


Figure 7. Diode clamped inductive load schematic

In figure 7 the equivalent circuits of the MOSFET with turn on divided into four periods at the diode clamped inductive load schematic is shown.

Figure 7 (a) equivalent circuit of period $t_0 \sim t_1$ in figure 6
Figure 7 (b) equivalent circuit of period $t_1 \sim t_2$ in figure 6
Figure 7 (c), (d) equivalent circuit of period $t_2 \sim t_3$ in figure 6
Figure 7 (d) equivalent circuit of period t_3 in figure 6

$t_0 \sim t_1$:

As i_G charges C_{GS} and C_{GD}, V_{GS} increases from 0 V up to $V_{GS(th)}$. The graph of increasing $V_{GS}(t)$ seems to be increasing linearly, but it is in fact an exponential curve having a time constant of

$$\tau_1 = R_G \cdot (C_{GS} + C_{GD1})$$

As shown in figure 7 (a), V_{DS} is still equal to V_{DD}, and i_D is zero. The MOSFET is still in the turn off state.

$t_1 \sim t_2$:

V_{GS} increases exponentially passing $V_{GS(th)}$, and as V_{GS} continues to increase, i_D begins to increase according to the linearized transfer curve shown in figure 4 and reaches full load current I_O. The time required for i_D to build up from zero to I_0 is the current rise time t_{ri}. When i_D is smaller than I_O, and when it is in a state where the free wheeling diode D_F is being conducted, V_{DS} maintains the V_{DD}.

$t_2 \sim t_3$:

Once the MOSFET is carrying the full load current I_0 but is still in the active region, V_{GS} becomes temporarily clamped to V_a which is the gate source voltage from the transfer curve of figure 4 needed to maintain $i_D = I_0$. V_a varies in accordance with the value from I_0. The entire gate current i_G, which is given by

$$i_G = \frac{V_{GG} - V_a}{R_G}$$

can only flow through C_{GD1}, as is indicated in figure 7(c). So the drain source voltage V_{DS} can be configured as the following ratios.

$$\frac{dv_{DG}}{dt} = \frac{dv_{DS}}{dt} = \frac{i_G}{C_{GD1}} = \frac{V_{GG} - V_a}{R_G \cdot C_{GD1}}$$

When V_{DD} increases (higher supply voltage), $t_2 \sim t_3$ the flat region of V_{GS} also increase.

At t_3 the drain source voltage V_{DS} becomes

$$V_{DSon} = I_0 \cdot r_{DS(on)}$$

and the transient is completed. The MOSFET is placed at the boundary of entering the ohmic region from the active one.

$t_3 \sim t_4$:

It is the period where the drain source voltage has completed its drop to the on state value and the gate source voltage V_{GS} becomes unclamped and continues its exponential growth to V_{GG}. This part of the growth occurs with a time constant

$$\tau_2 = R_G \cdot (C_{GS} + C_{GD2})$$

and simultaneously the gate current decays toward zero with the same time constant as is shown in the waveforms of figure 6.

2.1.4 Frequency response of the power MOSFET

The frequency response of the power MOSFET is limited by the charging and discharging of the input capacitance. If the C_{GS} and C_{GD} which determine the input capacitance become smaller, it is possible to work in high frequency. As the input capacitance is unrelated to the temperature, the MOSFETs switching speed is also unrelated to the temperature.

3 MOSFET Gate Driver

The primary function of a drive circuit is to switch a MOSFET from the off state to the on state and vice versa. The drive circuit for a power MOSFET will affect its switching behavior and its power dissipation. In most situations the designer seeks a low cost drive circuit that minimizes the turn on and turn off times so the MOSFET spends little time in traversing the active region where the power dissipation is large. Consequently the type of drive circuitry depends upon the application.

The signal processing circuits that generate the logic level to turn the MOSFET on and off are not considered part of the driver circuit. The drive circuit is the interface between the control circuit and the power switch. The drive circuit amplifies the control signals to levels required to drive the power switch and provides electrical isolation when required between the power switch and the logic level control circuits.

3.1 Half bridge power stage

The two fundamental categories for gate drivers are high side and low side. High side means that the source from the MOSFET can float between ground and the high voltage power rail. Low side means that the source is always connected to ground [D03]. An example of both of these types can be seen in a half bridge topology, shown in figure 8.

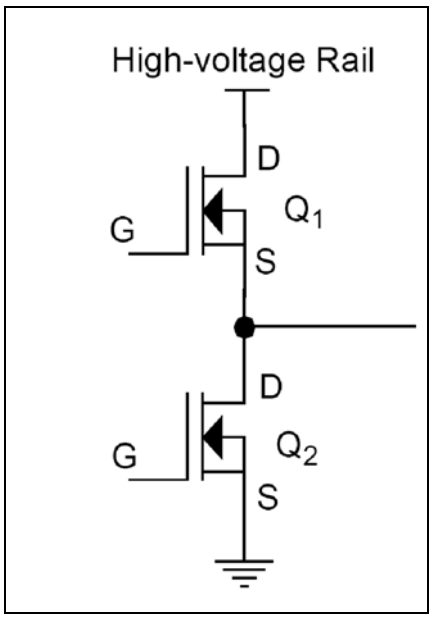


Figure 8. Example of a high side (Q_1) and low side (Q_2) gate drive requirement

In this configuration, Q1 and Q2 are always in opposite states. When Q1 is on, Q2 is off and vice-versa. When Q1 goes from being off to on, the voltage at the source of the MOSFET

goes from ground up to the high-voltage rail. This means that the voltage applied to the gate must float up as well. This requires some form of isolated, or floating, gate drive circuitry. Q2, however, always has its source connected to ground so the gate drive voltage can also be referenced to ground. This makes the gate drive at the low side much more simple.

3.2 High side gate driver

Various schemes exist for high side gate drive applications. These include floating gate drive supply designs, gate drive pulse transformers, charge pump drivers, high voltage bootstrap drive circuits, and carrier drive designs. Examples of these drive schemes and their key features are shown in table 1. Each basic circuit can be implemented in a wide variety of configurations.

Researching the gate drive circuitry listed in table 1 concluded, that the efficiently system in cost, complexity (number of components), security functions (integrated shutdown), reliability (MTBF, fit) [WIKI01] of the drive circuits will be a monolithic half bridge gate driver IC. Such MOSFET gate drivers (MGDs) integrate most of the functions required to drive a high side switch in a compact, high performance package. With the addition of few components, they provide very fast switching speeds up to few nanoseconds, a propagation delay between input command and gate drive output of some ten nanoseconds, a latched shutdown function, low power dissipation etc. This MGDs operate on the bootstrap principle or with additional floating power supply.

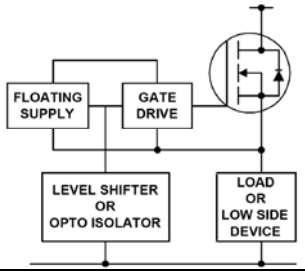
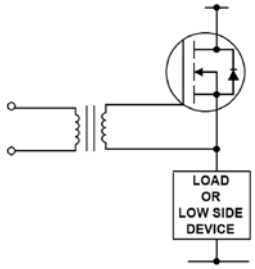
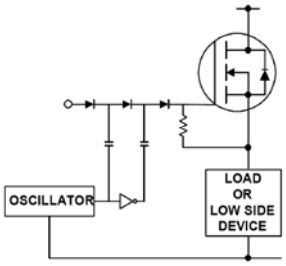
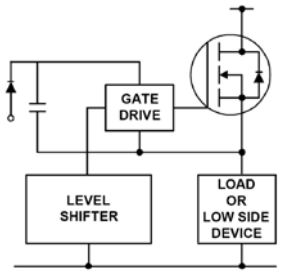
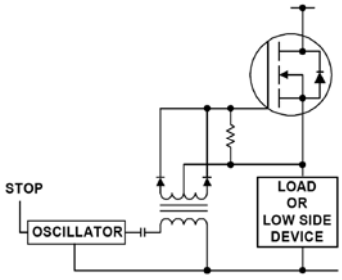
METHOD	BASIC CIRCUIT	KEY FEATURES
FLOATING GATE DRIVE SUPPLY		Full gate control for indefinite periods of time. Cost impact of isolated supply is significant. Level shifting a ground referenced signal can be tricky: Level shifter must sustain full voltage, switch fast with minimal propagation delays and low power consumption. Opto isolators tend to be relatively expensive, limited in bandwidth and noise sensitive.
PULSE TRANS-FORMER DRIVE		Simple and cost effective but limited in many respects. Operation over wide duty cycles requires complex techniques. Transformer size increases significantly as frequency decreases. Significant parasitic create less than ideal operation with fast switching waveforms.
CHARGE PUMP DRIVE		Can be used to generate an over rail voltage, controlled by a level shifter or to pump the gate when the MOSFET is turned on. In the first case the problems of a level shifter have to be tackled. In the second case turn on times tend to be too long for switching applications. In either case, the gate can be kept on for an indefinite period of time. Inefficiencies in the voltage multiplication circuit may require more than two stages of pumping.
BOOTS-TRAP DRIVE		Simple and inexpensive with some of the limitations of the pulse transformer: Duty cycle and on time are both constrained by the need to refresh the bootstrap capacitor. If the capacitor is charged from a high voltage rail, power dissipation can be significant. Requires level shifter, with its associated difficulties.
CARRIER DRIVE		Gives full gate control for an indefinite period of time but is somewhat limited in switching performance. This can be improved with added complexity.

Table 1. Several techniques to realize a MOSFET high side driver

3.2.1 Bootstrap Circuit

The bootstrap supply is formed by a diode and a capacitor connected as in figure 9. This method has the advantage of being simple and low cost but may force some limitations on duty cycle and on time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations [MRG04].

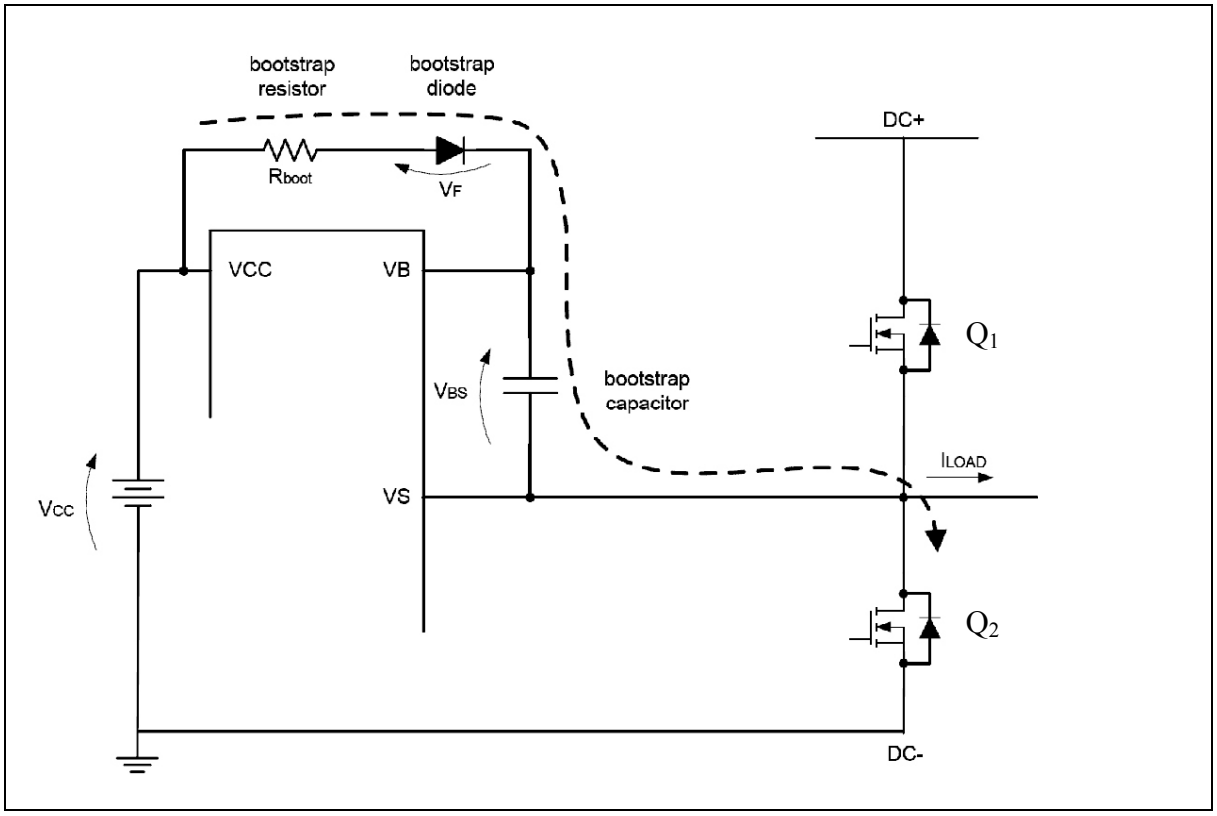


Figure 9. Bootstrap supply schematic

During the on time of Q_2, the source of Q_1 is at ground potential. This allows the bootstrap capacitor to be charged through the bootstrap diode from the bias supply voltage V_{CC}. When Q_2 is turned off and Q_1 is turned on, the voltage at the source of Q_1 begins to rise. The bootstrap capacitor now act as the bias source for the high side drive portion of the driver and provides the current to charge the gate of Q_1. The level shifting circuitry of the driver IC allows the high side drive stage to float up with the source voltage of Q_1. These types of drivers are often rated to handle up to 600 V (with respect to ground) on the high side drive portion of the circuitry. One of the draw backs to many of these types of driver is the long propagation delay time between the input signal and the high side drive turning on or off. This is a result of the level shifting circuitry. This can cause problems for some higher frequency applications as the delay times take up too much of the overall period. Though, for most power applications that are operating below 50 kHz, it is not an issue.

4 MOSFET Gate Driver ICs (MGD)

The given specification for the selection criteria of the MGD is to drive a half bridge power MOSFET stage with the data listed below:

Rail voltage $V_R = 96\ V_{DC}$
Nominal drain current $I_D = 15\ A_{DC}$
Maximal drain current $I_{Dmax} = 30\ A_{DC}$

A vary of MGDs exists on the market. Some MGDs can drive only one high side power device. Others can drive one high side and one low side power device. Others can drive a full three phase bridge. It goes without saying that any high side driver can also drive a low side device. Those MGDs with two gate drive channel can have dual hence independent input commands or a single input command with complementary drive and predetermined dead time. For the given definition a half bridge gate driver IC with two independent inputs for the high and the low side will be the best solution. But which part and manufacturer should be implemented?

A lot of semiconductor companies are developing and producing MGDs. By researching the internet the following manufacturers amongst others have been found for MGD products:

- FAIRCHILD Semiconductor Corporation
- Infineon Technologies
- International Rectifier
- Maxim Integrated Products
- Microchip Technology
- National Semiconductor
- SEMIKRON
- STMicroelectronics
- Vishay Siliconix

This manufacturers offer a lot of different devices. To choose the right part is the job of the circuit designer. We decided to take a device from International Rectifier. The selection criteria on this will be described in the next chapter.

4.1 Selection criteria on MGDs

Figure 10 shows a typical connection of MGD in a half bridge circuit with internal level shifting and external bootstrap components (D1 and C1).

The Logic Inputs HIN (high side in), LIN(low side in) and SD(shut down) are compatible with standard CMOS or LSTTL outputs [IRF05].

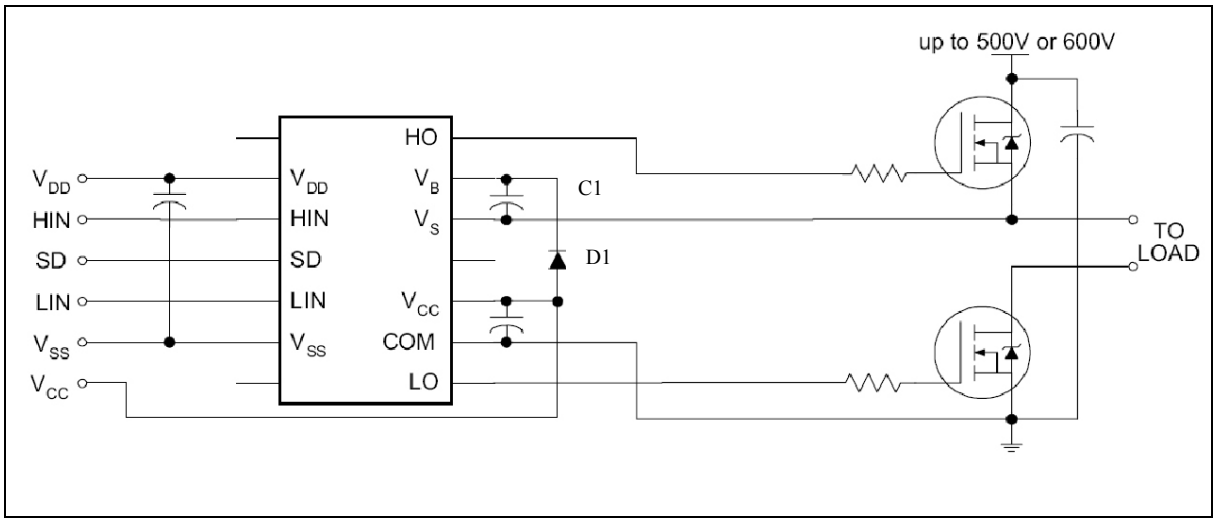


Figure 10. Typical connection of a MGD

For a better explanation on the technical specification of MGDs figure 11 shows a functional block diagram of a half bridge gate driver IC with two independent inputs for the high and the low side and a shut down function for e.g. external over current detection in the half bridge stage.

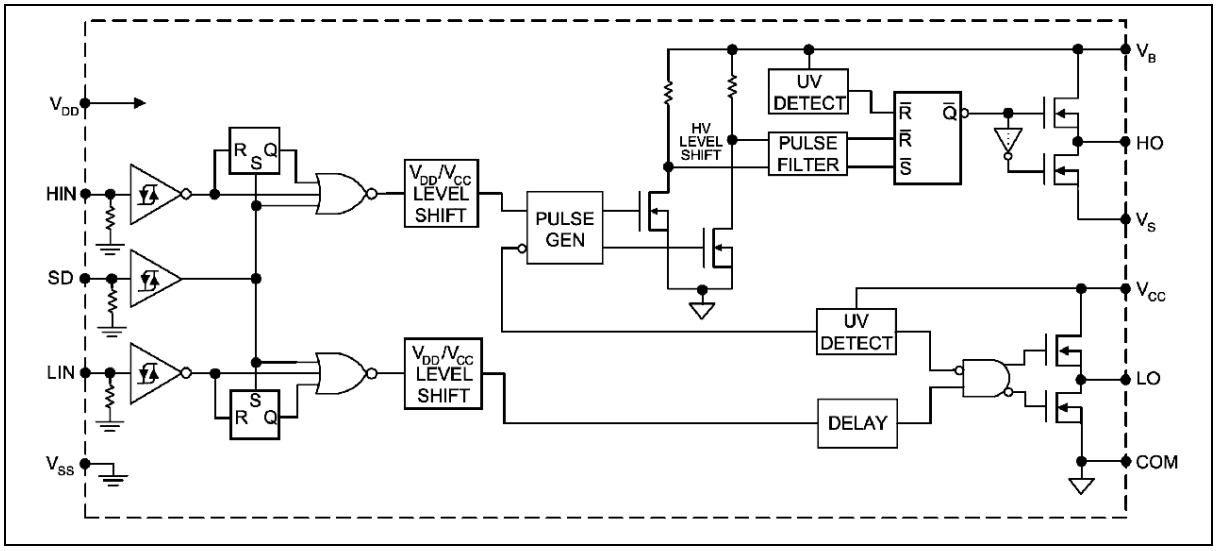


Figure 11. Functional Block Diagram of a MGD

The block diagram in figure 11 shows, the internal functional structure of the IC, such as the pull down resistors and the Schmitt trigger on the input pins, the shut down logic, the level shift circuits (V_{DD} ➔ V_{CC} and V_{CC} ➔ V_B), the under voltage detect (UVLO) for high and low side supplies, the time delay for the low side to match the same timing between high and low side and the transistor output stage for both sides.

The following listed specifications were the basis for the selection of our device. In the technical datasheets the figures and values provide detailed characterization of various specifications such as the variation of turn on time with temperature, shutdown time with respect to V_{DD} supply voltage, junction temperature with respect to switching frequency, etc. Most figures show the variation of the maximum and typical values of the given specification. This helps the designer to utilize the IC to its full potential.

4.1.1 High side floating supply voltage V_B and offset voltage V_S

This is the maximum voltage at the V_B pin with respect to the COM in figure 11. MGDs are often rated to handle up to 600 V (with respect to ground) on the high side drive. This value represents the maximum voltage in the circuit system. The absolute maximum rail voltage of the half bridge in figure 10 is about 25 V below. V_S the high side floating supply offset voltage is the maximum swing allowable at the V_S pin, with respect to V_B. Normally it is between V_B + 0.3 V (maximum), and V_B – 20 V (minimum).

4.1.2 Low side supply voltage V_{CC}

This is the supply voltage at the V_{CC} pin in figure 11, which provides the biasing power supply for the low side channel.

4.1.3 Logic supply voltage V_{DD}

This is the supply voltage at the V_{DD} pin in figure 11 providing biasing to the input side circuit of the IC, and is referenced to the V_{SS} pin (ground).

4.1.4 Turn on propagation delay t_{ON}

This is the time taken for the output voltage at HO or LO to reach to 10% of its maximum possible value, when the input has reached 50% of its maximum possible value. The switching time waveforms definition is shown in figure 12. It essentially reflects the delay between the time when a signal is applied at the input HIN or LIN, to the time the output starts going high at HO or LO.

4.1.5 Turn off propagation delay t_{OFF}

This is the time taken for the output voltage at HO or LO to reach to 90% of its maximum possible value, when the input has reached 50% of its maximum possible value. It essentially reflects the delay between the time when a signal is applied at the input HIN or LIN, to the

time the output starts going low at HO or LO. The switching time waveforms definition is shown in figure 12.

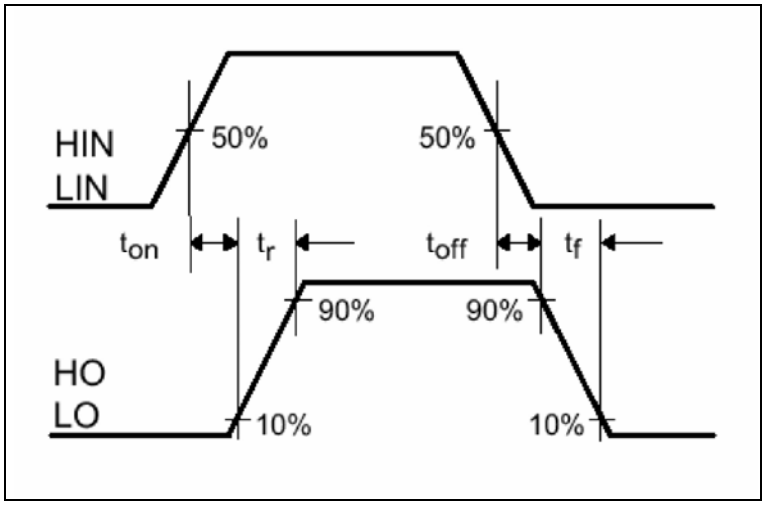


Figure 12. Switching time waveforms definition

4.1.6 Shutdown propagation delay t_{SD}

This is the time taken for the outputs at HO and LO to decrease to 90% of their maximum values, when the signal at the shutdown input (SD pin) has reached 50% of its maximum value. The shutdown waveform definition is shown in figure 13.

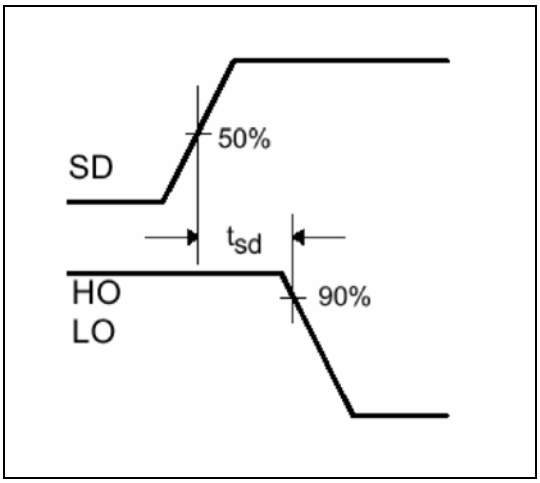


Figure 13. Shutdown waveform definition

4.1.7 Turn on rise time t_r

This is the time taken for the outputs HO and LO to reach 90% of their maximum values. The shorter the rise time, the faster is the IC response. The switching time waveforms definition is shown in figure 12.

4.1.8 Turn off fall time t_f

This is the time taken for the outputs HO and LO to reach 90% of their maximum values. Again, the shorter the fall time, the faster is the IC response. The switching time waveforms definition is shown in figure 12.

4.1.9 Delay matching high side and low side turn on and turn off MT

This is the time difference between the LO and HO outputs, when each output has reached 10% of it's maximum during turn on, or when each output has decreased to 90% of it's maximum during turn off, assuming that HIN and LIN are simultaneously applied. The delay matching waveforms definition is shown in figure 14. The shorter the delay matching time, the better the circuit performance.

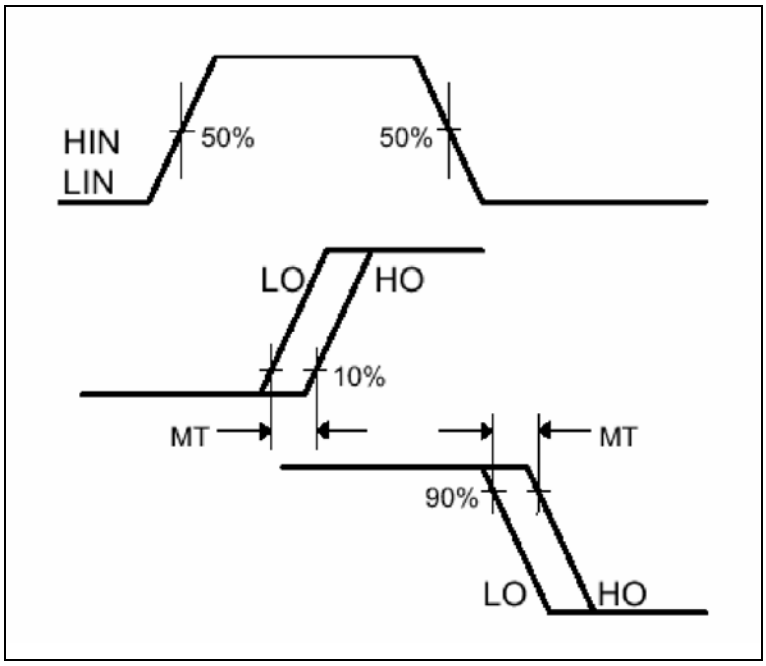


Figure 14. Delay Matching waveforms definition

4.1.10 Output high short circuit pulsed current I_{O+}

This is the peak current that can flow out of the output pins, for a given pulse duration, when the respective input pin is high, and the output pin is shorted to the COM. This represents the peak capacity of the IC to supply the gate charge of the driven switch.

4.1.11 Output low short circuit pulsed current I_{O-}

This is the peak current that can flow into the output pins, for a given pulse duration, when the respective input pin is low, and the output pin is fully biased with respect to the COM. This represents the peak capacity of the IC to discharge the gate charge of the driven switch.

4.1.12 Price per device

The budgetary pricing of 1000 pieces.

4.2 Selection Table

Part	Datasheet	VS [V]	VCC Range [V]	VDD [V]	ton [ns]	toff [ns]	tSD [ns]	tr [ns]	tf [ns]	MT [ns]	IO+ [mA]	IO- [mA]	1K Price [USD]
IR2010	ir2010.pdf	200	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	95	65	70	10	15	15	3000	3000	1.875
IR2011	ir2011.pdf	200	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	80	60	NO SD	35	20	20	1000	1000	1.562
IR2101	ir2101.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	160	150	NO SD	100	50	50	100	210	1.500
IR2106	ir2106.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	220	200	NO SD	150	50	50	120	250	1.650
IR2110	ir2110.pdf	500	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	120	94	110	25	17	10	2000	2000	2.438
IR2112	ir2112.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	125	105	105	80	40	30	200	420	1.650
IR2113	ir2110.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	120	94	110	25	17	20	2000	2000	2.750
IR2181	ir2181.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	180	220	NO SD	40	20	35	1700	1700	1.875
IR2213	ir2213.pdf	1200	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	280	225	230	25	17	30	1700	2000	4.375
IR2301	ir2301.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	220	200	NO SD	130	50	50	120	250	1.250
IRS2101PBF	irs2101.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	160	150	NO SD	70	35	50	100	210	1.175
IRS2106	irs2106.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	220	200	NO SD	100	35	30	290	600	1.312
IRS2110PBF	irs2110.pdf	500	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	130	120	130	25	17	10	2000	2000	1.800
IRS2113PBF	irs2110.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	130	120	130	25	17	20	2000	2000	2.013
IRS2181	irs2181.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	180	220	NO SD	40	20	35	1400	1800	1.500
IRS2186PBF	irs2186.pdf	600	(10 - 25)V with undervoltage lockout	(3 - 20)V CMOS + TTL compatible	170	170	NO SD	22	18	35	4000	4000	1.750

Table 2. IRF Monolithic MOSFET gate driver selection table

4.3 Selected Device

The selection on the listed MGD in table 2 was made on the criteria, explained in chapter 4.1. Because of the fast switching speed, the very short propagation delay, the high output current and the shut down function the MGD IRS2113PBF was selected. The key features are listed below:

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Under voltage lockout for both channels
- 3.3 V logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground ± 5V offset
- CMOS Schmitt triggered inputs with pull down
- Cycle by cycle edge triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant

A full bridge power stage circuit with the monolithic IC IRS2113PBF as MOSFET gate driver for the two low side switches has been tested. The next chapter shows the circuit and the test result.

5 Power stage test circuit and measurement report

The following chapter shows the test results of the measurements which have been made on the self made evaluation test board. Figure 15 shows the test equipment. The power stage was designed to drive a dc motor. As control unit a development board from an early project with a PIC 16F877A was taken. The Software was written in C and realizes the turn on and off commands.

The following measure and additional equipment was used:

- Self made evaluation board power stage, shown in figure 18 and 19
- dc motor (EPH Elektronik) $U_N = 24V$, $I_N = 10A$
- logic and control unit LPVT_CMP06P A&R TECH GMBH (PIC16F877A)
- DC power supply (30V/100A) DELTA SM30-100D
- Oscilloscope TEK3032 (2 channel, 300MHz 2,5GS/s)
- Test Probe (passive) TEKP6139A (500MHz, 10MOhm, 8pF, 10x)
- Current Probe FLUKE 80i-110s AC/DC ($I_{max} = 100A$)
- LCR Meter GW INSTEK LCR816

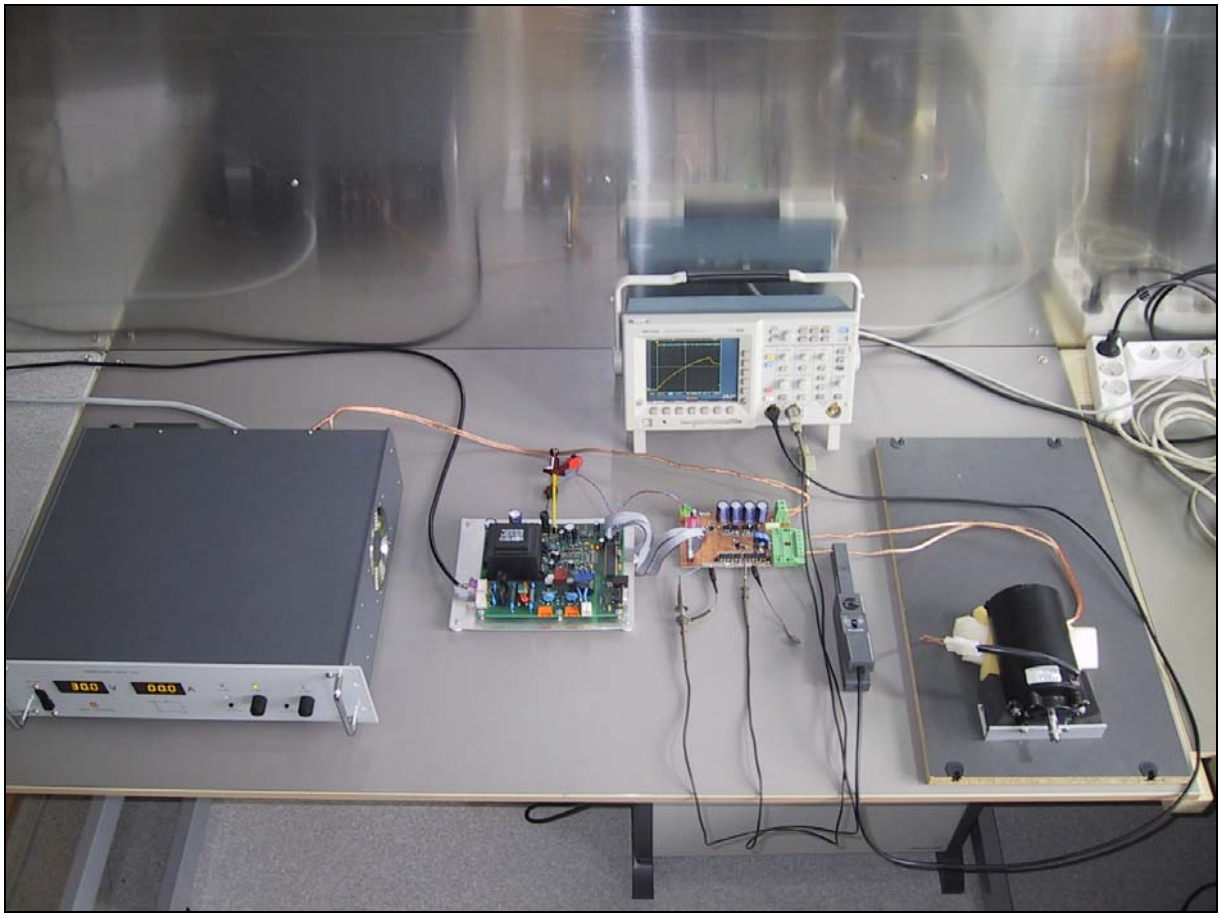


Figure 15. Full bridge power stage test design

5.1 Circuit and measurement description

In figure 16 the whole circuit from the test board is shown. The high side switches were realised with a BTS660P from Infineon. This is a n channel vertical power FET with charge pump, current controlled input and diagnostic feedback with load current sense, integrated in Smart SIPMOS chip on chip technology providing embedded protective functions. In the low side the VNB35N07 from ST Microelectronics is implemented. This transistor is a monolithic device using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Both power MOSFETs are internal fully auto protected (thermal shutdown, short circuit protection, etc.).

In this design the power stage is galvanic isolated from the control unit. This is realized by a ADUM1100 from Analog Devices. This part is a digital isolator based on iCoupler technology. Combining high speed CMOS and monolithic air core transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives, such as optocoupler devices. The propagation delay is smaller than 18 ns and is compatible with temperatures up to 125°C. It operates at very low power, less than 0.9 mA of quiescent current (sum of both sides), and a dynamic current of less than 160 μA per Mbps of data rate. Unlike other optocoupler alternatives, the ADuM1100 provides dc correctness with a patented refresh feature that continuously updates the output signal.

For the driver circuit power supply a dc to dc converter TEN5-2413 from TRACO was used.

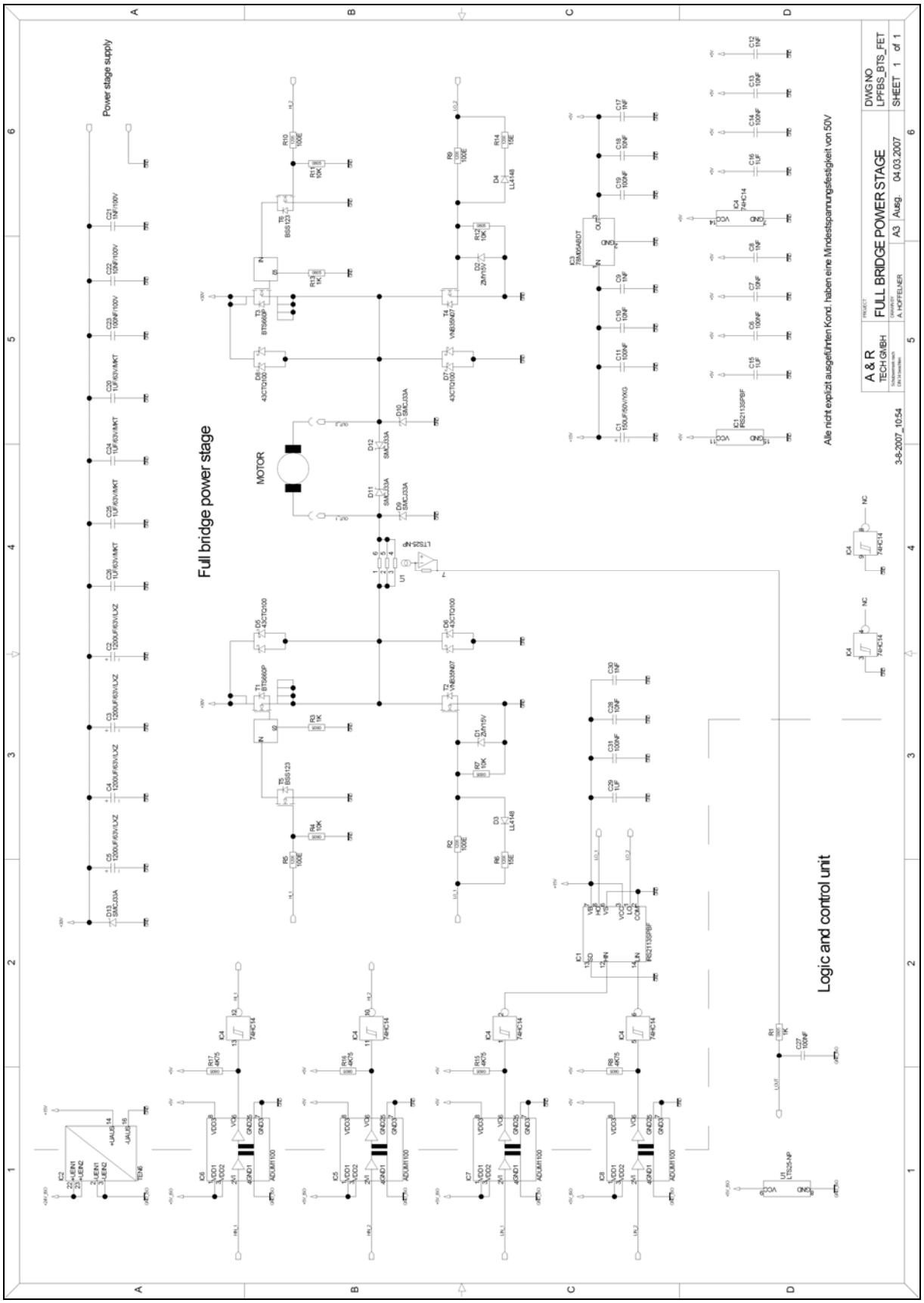


Figure 16. Schematic of the full bridge power stage

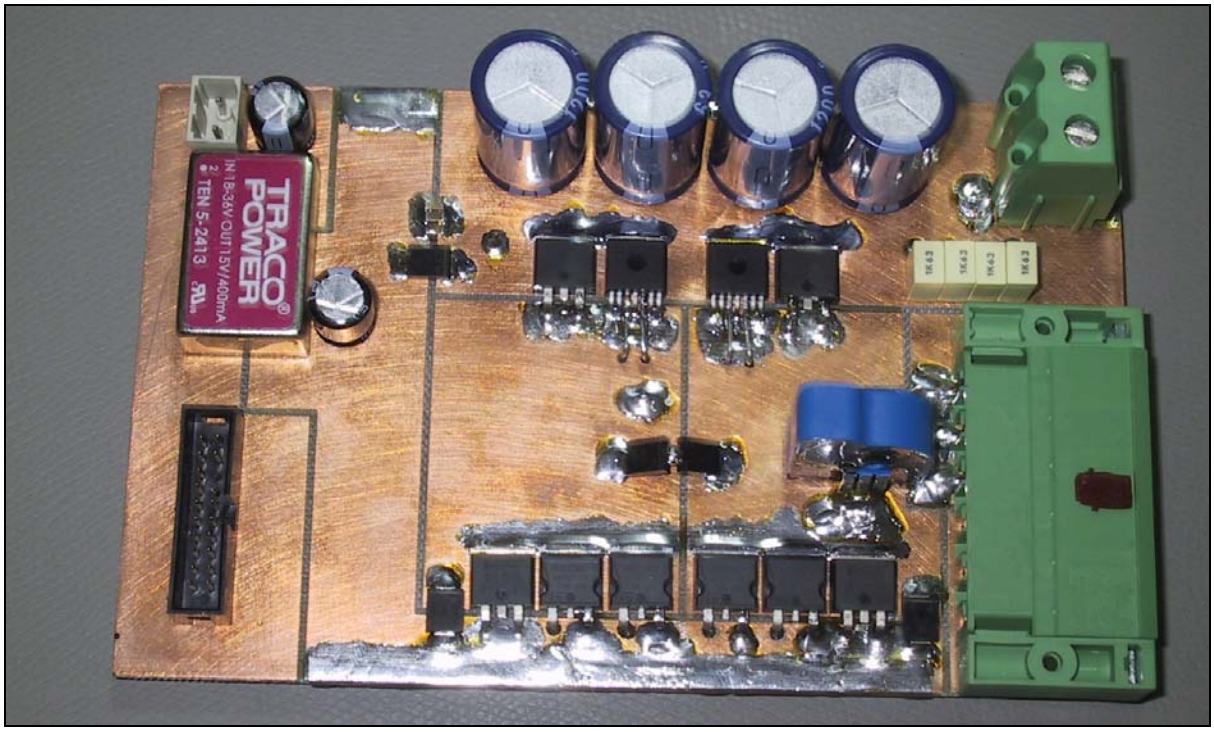


Figure 17. Top view of the full bridge power stage print circuit board

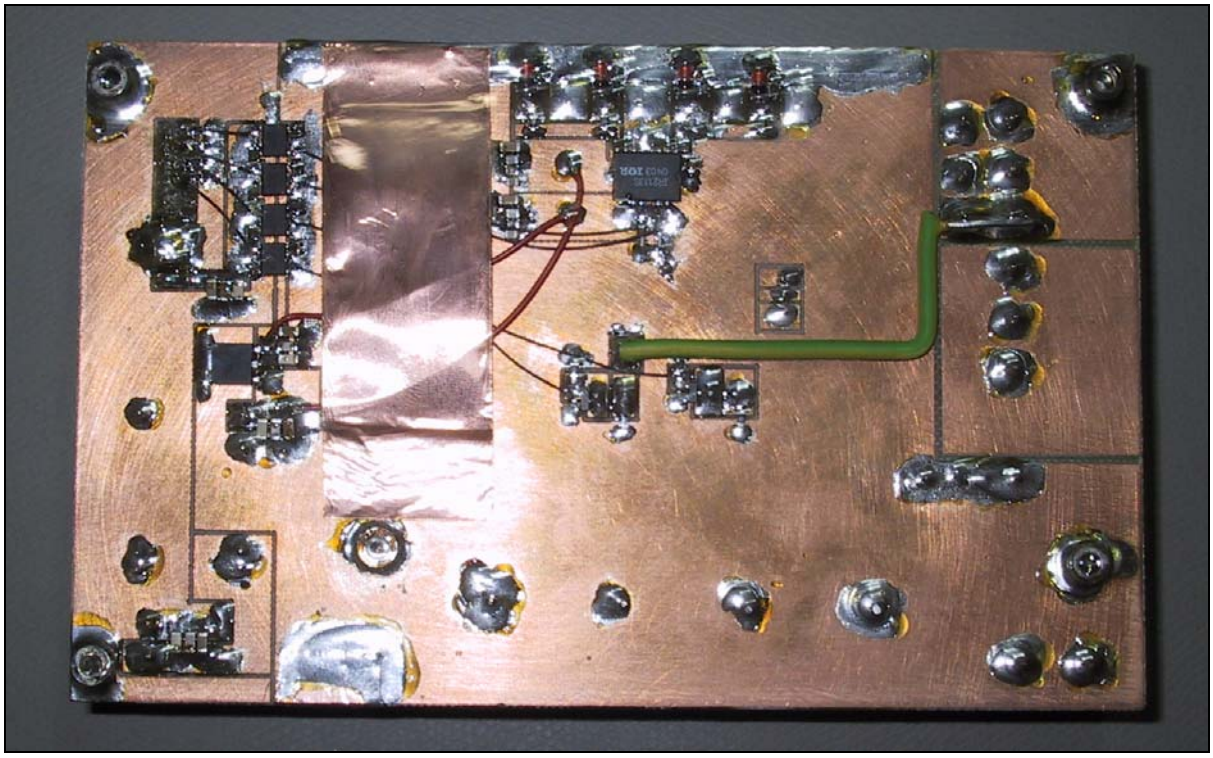


Figure 18. Bottom view of the full bridge power stage print circuit board

5.2 Measurement result

In the following chapter the measurement results and switching waveforms during turn on and off the low side MOSFET VNB35N07 is documented. Only one driver output from the MGD was measured.

The following figure 19 shows a small section from the schematic in figure 16. Here the points were the measurements on the development board have been done were marked.

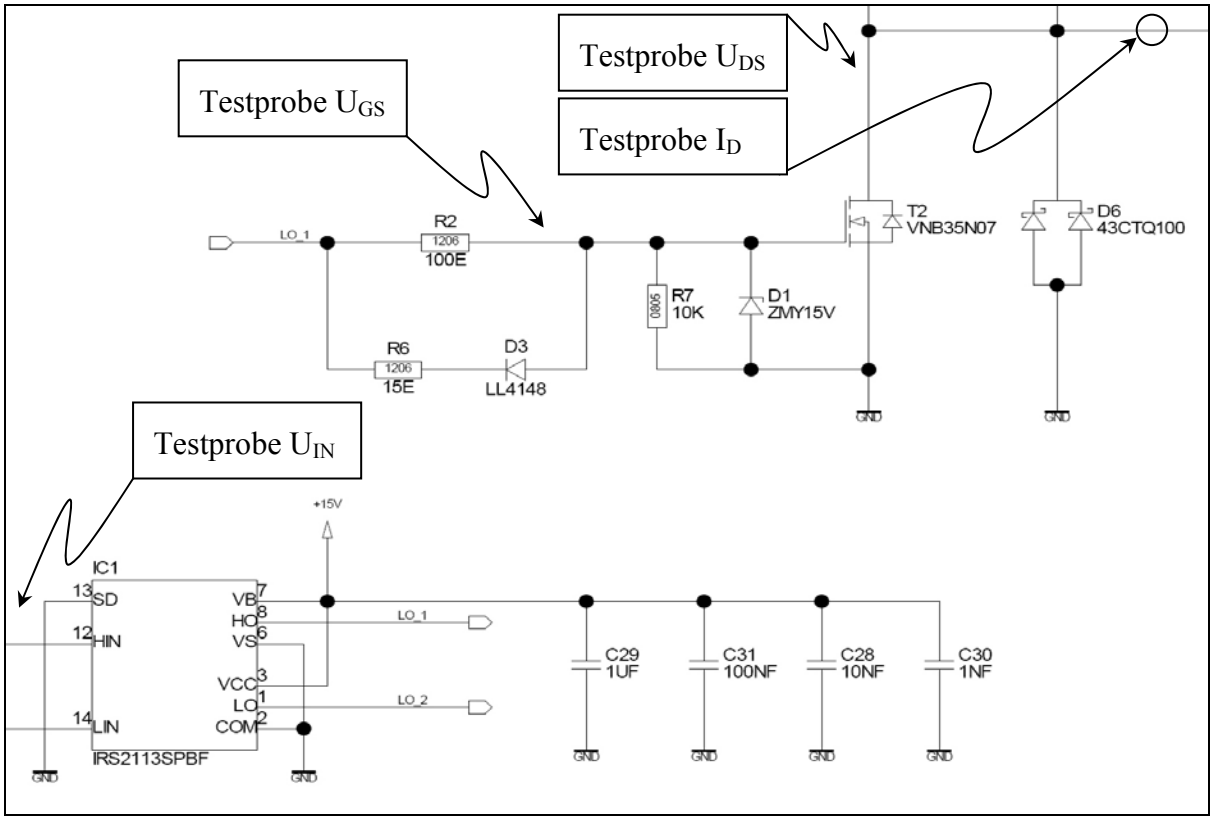


Figure 19. Measurement points

Due to fast switching capabilities e.g. the rise time t_R = 3ns, the measuring probe with the standard GND cable gives not the correct result. In the technical literature such GND cables are called pigtail [WIKI02]. The disassembled test probe to measure the correct signals is shown in figure 20. At this position U_{GS} from the low side MOSFET VNB35N07 was measured.

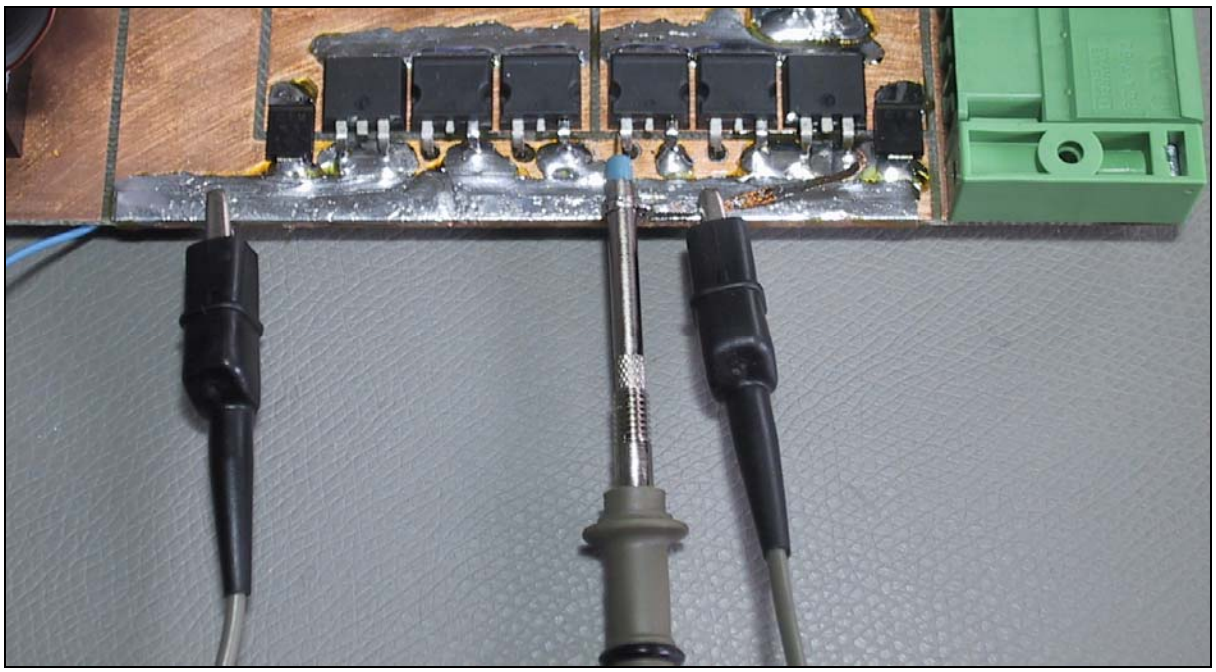


Figure 20. Disassembled voltage test probe with a "good" GND connection to the test board

Figure 21 and 22 shows the propagation delay from the MOSFET gate driver during turn on and off. The correct high side switch T3 was the whole time in the on state. U_{IN} was generated from the control unit. The measurement result shows that the specified propagation delay from the datasheet is almost too long.

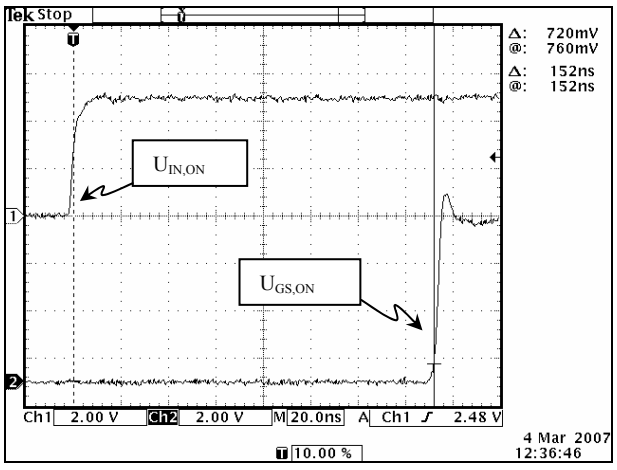


Figure 21. Turn on propagation delay t_{ON}

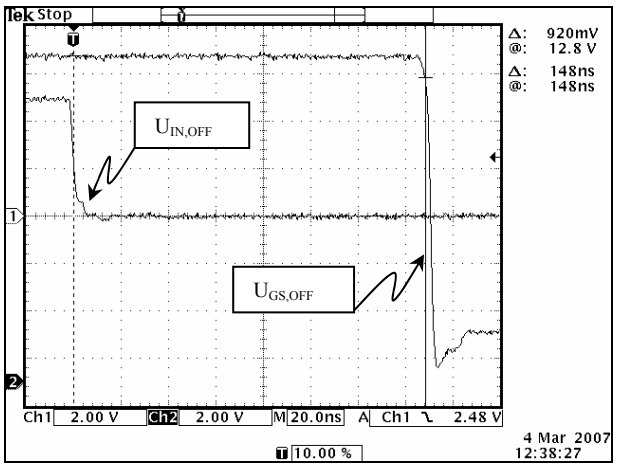


Figure 22. Turn off propagation delay t_{OFF}

To measure the correct turn on and turn off rise and fall time from the MOSFET gate driver the development board was modified. The driver output was disconnected from the rest of the circuit. Now this pin was connected over a 7,5 Ω resistor (two 15 Ω paralleled) direct to GND. The supply voltage from the MGD was 15 V. This action ensured that the output stage has to drive a defined current. Here we assume that the impedance from our resistor is ohmic and the parasitic inductance and capacitance are very low. The measured waveforms can be seen in figure 23 and 24. It was positive surprising that the rise (3,156 ns) and fall time (2,956 ns) was shorter than the given time in the MGDs datasheet.

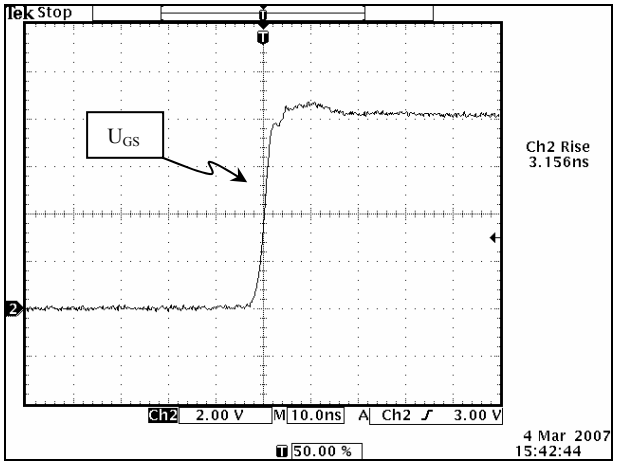


Figure 23. Turn on rise time t_r

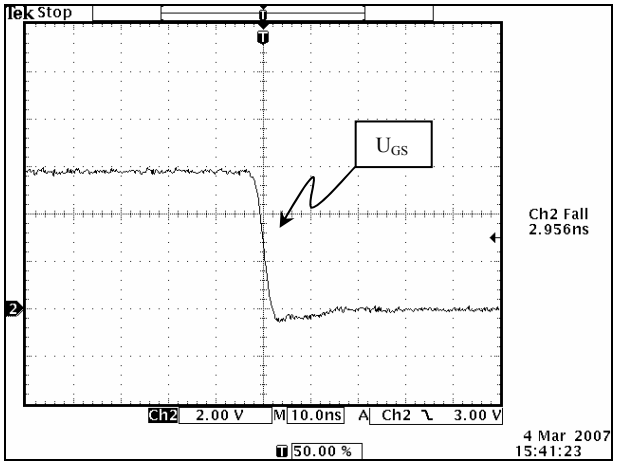


Figure 24. Turn off fall time t_f

In figure 25 and 26 the gate source and drain source voltage during turn on was measured. Here the theoretical background from chapter 2 could be verified. The miller plateau could be seen. and with the given gate resistor the specified gate charges from the MOSFET datasheet could be checked.

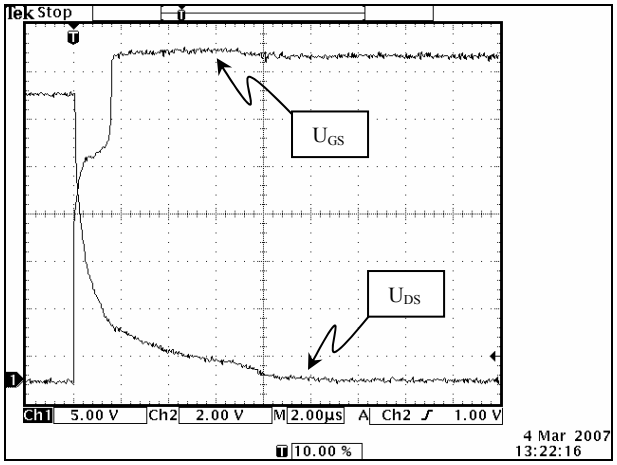


Figure 25. Turn on (x-axis = 2 µs / DIV)

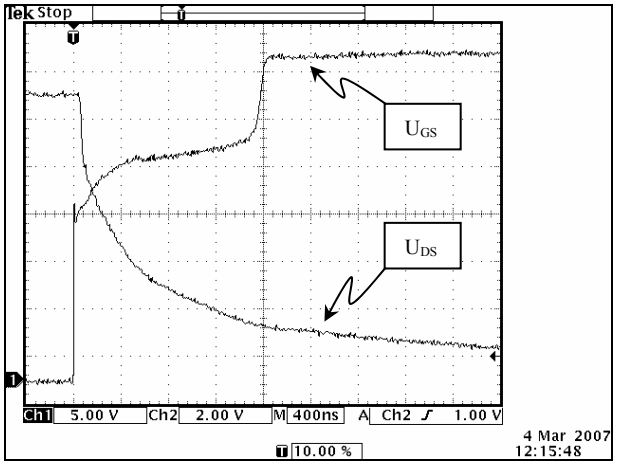


Figure 26. Turn on (x-axis = 400 ns / DIV)

The same measurement like before during turning off the MOSFET is shown in figure 27 and 28.

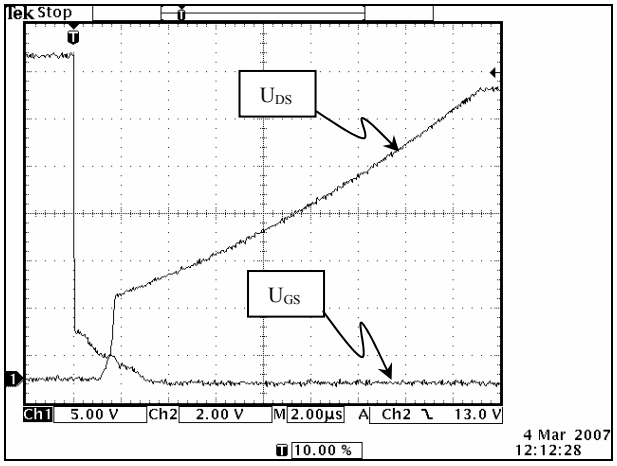


Figure 27. Turn off (x-axis = 2 µs / DIV)

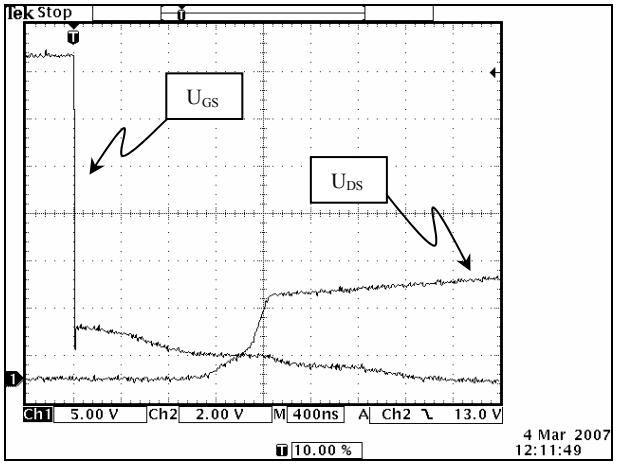


Figure 28. Turn off (x-axis = 400 ns / DIV)

In figure 29 and 30 the drain current is shown. At the output pins from the power stage a brush dc motor was connected. The maximum turn on current is about 50A. The current rise time is defined by the rotor inductance and limited by the rotor resistor. Figure 31 shows the measurement from this two factors. With this two parameters the same current rise time was calculated like the current shows in figure 29.

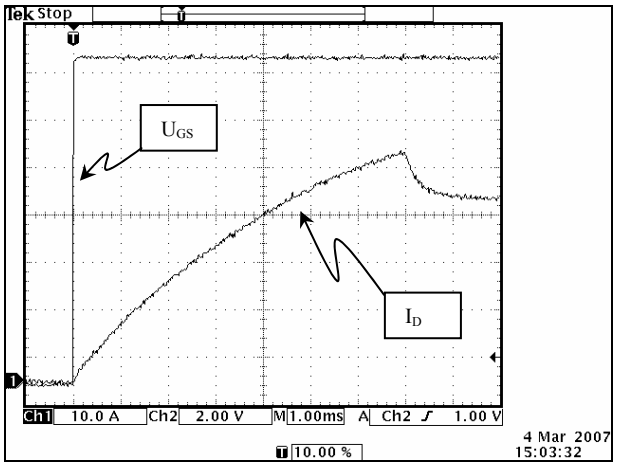


Figure 29. Turn on (x-axis = 1 ms / DIV)

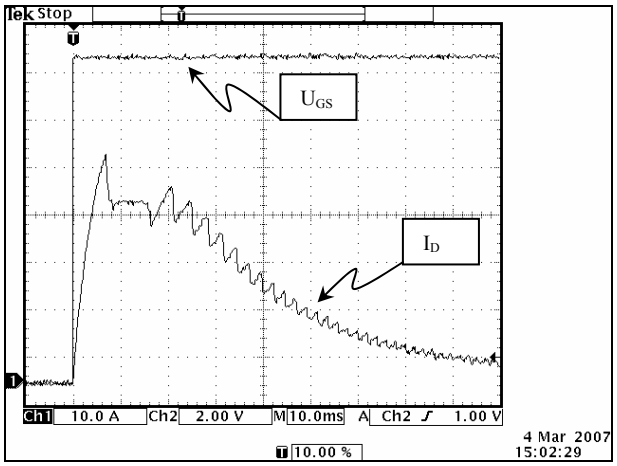


Figure 30. Turn on (x-axis = 10 ms / DIV)

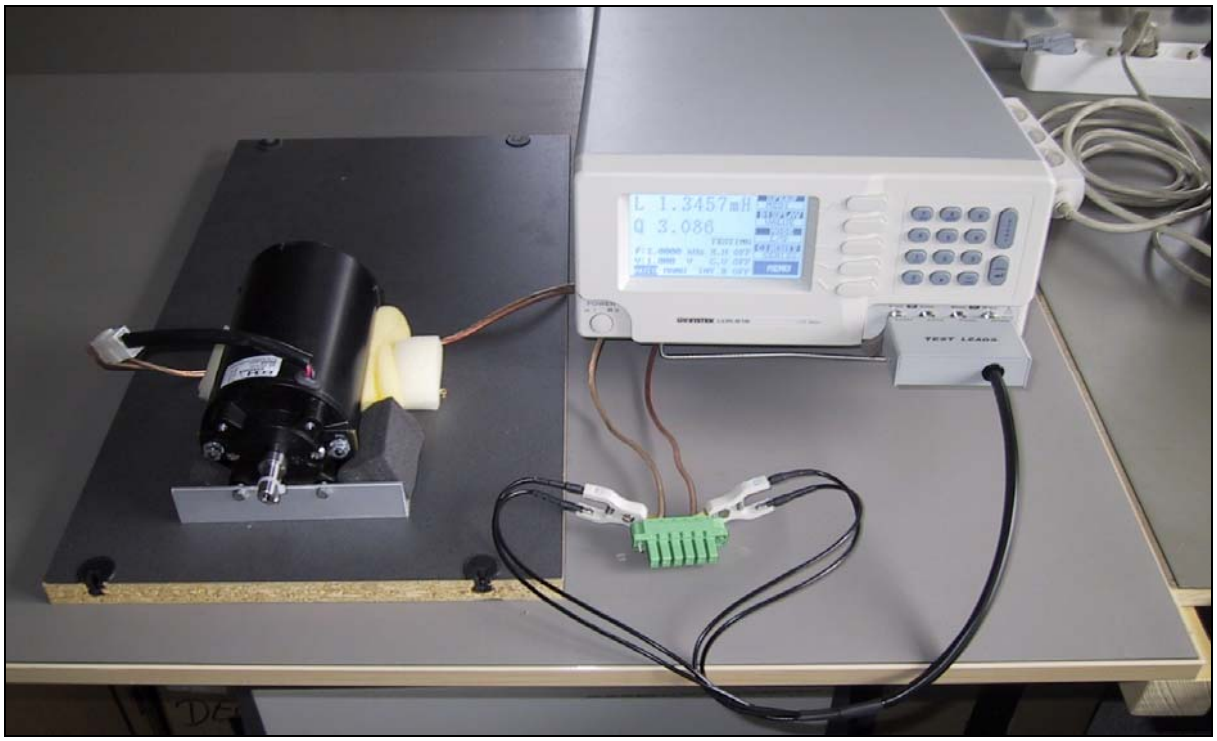


Figure 31. Measuring the rotor resistor and inductance from the dc brush motor

6 Conclusion

It was very interesting to get an overview on the huge concepts of MOSFET gate drivers. Because at the limited period of time only the main systems could be investigated. The online search for such systems has shown that the research and production on monolithic gate drivers is very sophisticated. To build up a driver stage for MOSFETs with exclusive discrete components would only in special applications be necessary. The measurements on the self made test board have shown that in our case the implementation of such an integrated monolithic circuit in a power MOSFET driver stage was the right decision. But we could also see, that the given specification from the semiconductor manufacturer are not always true. The propagation delay at room temperature almost exceeded the defined value. Also the correct selection at the additional components, described in the technical papers and specifications, are very necessary and have a huge positive or negative affect at the circuit result. Our measurements also have shown that at switching times around some nanoseconds and drain currents above fifty amperes the engineers standard equipment is at the limit. For such hardware developments a well equipped laboratory is necessary.

The next step on this work will be, to implement this driver circuit in a half bridge stage with big power MOSFETs. But this will be a new topic for a bachelor work.

7 Literature

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