Resolving the Mystery of Breakdown Failures caused by Passivation Damage

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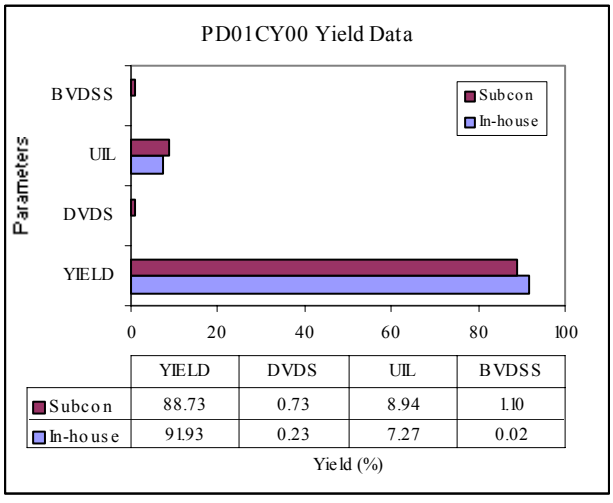
ABSTRACT

This paper will be discussing on how the root cause for test yield variances was determined between sites having the same products tested.

The problem was thought to be a die related problem since the same failure mode were seen at final test for both sites only the magnitude is higher at the subcontract facility. It turned out to be an assembly-related defect causing the same manifestation as the inherent product problem.

1. 0 INTRODUCTION

Yields at the subcontract site for TO263 MOSFETs (metal oxide semiconductor field effect transistor), during the first months of production, were ~5% below than Fairchild Cebu built lots. Both sites were experiencing UIL (Unclamped Inductive Load) failures which were traced to be limited by die capability. However, UIL and BVdss yield losses for subcon lots were abnormally higher than Cebu built lots.



	YIELD	DVDS	UIL	BVDSS
Subcon	88.73	0.73	8.94	1.10
In-house	91.93	0.23	7.27	0.02

Figure 1. Subcon yield data versus Cebu yield data.

1.1 Final Test Structure

Final test structure for MOSFET devices usually requires DVDS (delta Vds), UIL and DC (direct current) parametric testing.

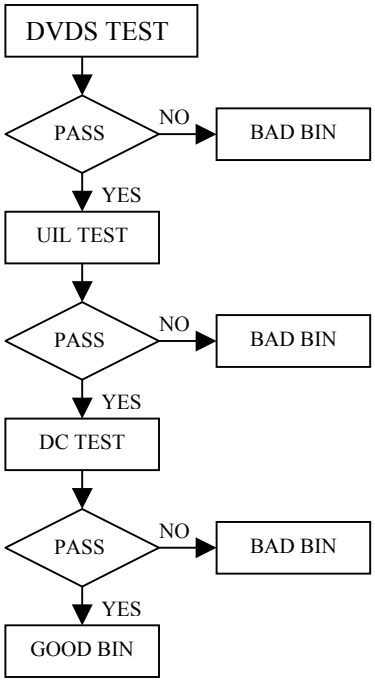


Figure 2. Final Test Structure.

The sequences of tests for FSC MOSFETs are dVDS, UIL and then DC. DVDS test will screen out functional failures since this will be the first test that the DUT (device under test) will encounter and die attach related failures such as voids. The UIL test is a product guarantee for robustness. This test is similar to resistive switching. They only differ in type of load and the magnitude of current applied. The DC tests are composed of parameters checking the static characteristics of the DUT. Common DC parameters for MOSFETs are BVdss, Vgsth, Igss, Idss, Rdson and Vsd. Ideally, DC tests should only encounter limit failures and not functional failures since these are already weeded out in the previous two tests.

1.2 Product UIL Problem

The device loaded for subcon has an inherent problem on UIL energy capability. Previous characterization showed that the product distribution is already marginal to the specified limits. UIL failures appear as a short circuit upon

DC verification and die visual analysis after package decapsulation will show EOS (electrical over-stress) footprints ranging from minute single or multiple cell damages to localized severe burn out. Analysis on these footprints showed that the failures did not withstand the applied energy causing some of the cells to latch up and eventually burnt out.

1.3 Subcon Cloud

Initial investigation on the low yield problem was clouded by the inherent product problem. Failure analyses done by subcon always show EOS failures during die visual examination. This is because the failure mode has the same mechanism as the inherent product problem and therefore will be classified by the test system as the same failure.

2.0 EXPERIMENTAL SECTION

2.1 Materials

Experiment vehicle device, subcon and in-house built assembly lots, DVDS tester, UIL tester, DC tester and handler.

2.2 Procedure

The same device loaded at subcon site was chosen to be the experiment vehicle. Untested lots from subcon and in-house builds were randomly chosen. There were 2 sets of experiments done. Experiment 1 was the yield comparison for in-house built lots versus subcon built lots tested in Cebu. Experiment 2 was composed of two splits. Split 1 lots were built at subcon while split 2 lots were built in Cebu (See table 1). All splits were tested in Cebu. DC testing was done first on Experiment 2 lots prior to the UIL test. Purpose was to screen out assembly related defects prior to UIL testing. This was also done to weed out assembly related defects that would skew the UIL data. All parametric tests were datalogged. DVDS test was omitted. Failures were sent to FA Laboratory for package decapsulation and internal visual inspection.

Table 1. Summary of Experiment Splits

Expt 1	Assy Site	Test Site	Test Sequence
Split1-1	Subcon	FSC	DVDS->UIL->DC
Split1-2	FSC	FSC	DVDS->UIL->DC
Expt 2	Assy Site	Test Site	Test Sequence
Split2-1	Subcon	FSC	DC->UIL
Split2-2	FSC	FSC	DC->UIL

3.0 RESULTS AND DISCUSSION

3.1 UIL failures or not???

Data for Experiment 1 showed that UIL and BVdss failures for subcon built lots were higher than FSC built lots (See table 2). Parametric datalog for subcon built lots on BVdss was also skewed to the left indicating an underlying problem that was not screened by the UIL test (See Figs 3 and 4).

Table 2. Yield Data for Experiment 1.

Expt 1	Split1-1	Split1-2
Qty	92522	180570
Bin1 (good)	87.41%	94.41%
Bin3 (Rds)	00.00%	00.10%
Bin4 (BVdss)	02.73%	00.32%
Bin6 (DVDS)	00.03%	00.01%
Bin7 (UIL)	09.84%	05.17%

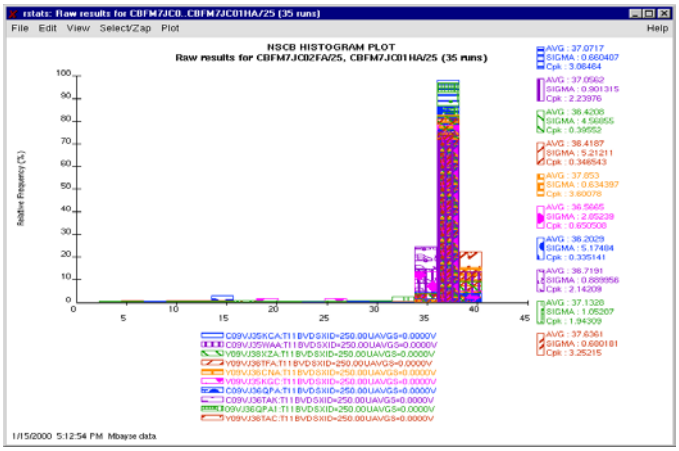


Figure 3. BVdss datalog for Split1-1 subcon built lots.

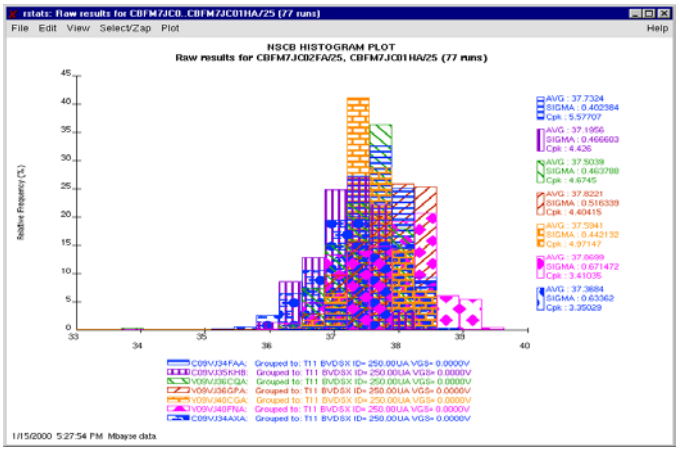


Figure 4. BVdss datalog for Split1-2 FSC built lots.

Data for Experiment 2 showed that the DC test yields for FSC built lots were significantly higher than subcon built lots. BVdss failures for subcon built lots were also abnormally high. The degree of UIL failures between the splits did not significantly differ. (See tables 3 and 4)

Table 3. Experiment 2 DC test yield data

Split2-1 DC Test Yield Data				
Lot #	Qty In	Yield	PreOS	BVdss
C010274990	894	90.83%	00.11%	08.17%
C010275003	910	93.96%	00.44%	05.60%
C010266867	927	90.18%	01.40%	07.55%
C010284885	1010	78.22%	01.68%	20.10%
C010275012	895	81.45%	01.01%	17.54%
Cum	4636	86.76%	00.95%	11.95%
Split2-2 DC Test Yield Data				
Lot #	Qty In	Yield	PreOS	BVdss
C010295829	1020	97.65%	02.16%	00.20%
C010294841	0999	98.90%	01.00%	00.10%
C010295802	1023	97.56%	01.37%	00.88%
C010297579	1033	97.68%	01.45%	00.87%
C010296965	1030	96.41%	02.43%	00.97%
Cum	5105	97.63%	01.68%	00.61%

Table 4. Experiment 2 UIL test yield data

Split2-1 UIL Test Yield Data				
Lot #	Qty In	Yield	UIL	%UIL
C010274990	812	97.04%	20	02.46%
C010275003	855	93.80%	53	06.20%
C010266867	836	85.17%	115	13.76%
C010284885	790	80.76%	149	18.86%
C010275012	729	69.82%	217	29.77%
Cum	4022	85.75%	554	13.77%
Split2-2 UIL Test Yield Data				
Lot #	Qty In	Yield	UIL	%UIL
C010295829	996	95.78%	29	02.91%
C010294841	988	96.05%	33	03.34%
C010295802	998	98.30%	16	01.60%
C010297579	1009	97.42%	15	01.49%
C010296965	993	70.80%	279	28.10%
Cum	4984	91.69%	372	07.46%

FA results of failures from BVdss failures from split2-1 showed excessive gate wire tail. Gate wire was already extending to the EQR (equi-potential ring) region, breaking the passivation and creating a resistive path between the gate wire and the guard ring. (See Figs 5 and 6)

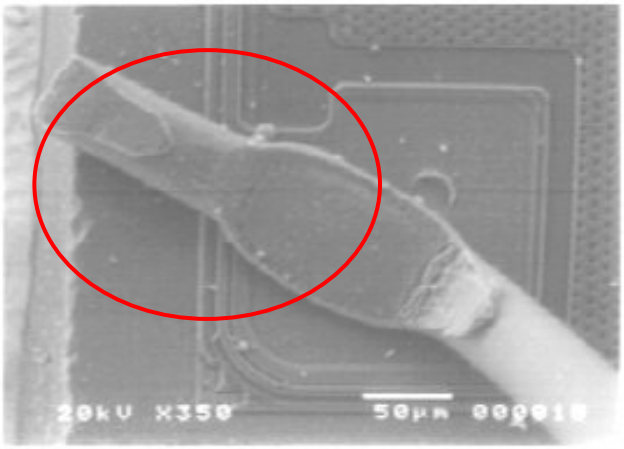


Figure 5. SEM photo of gate wire.

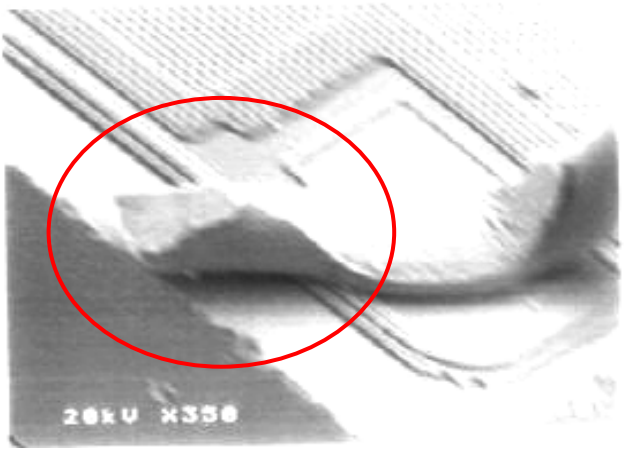


Figure 6. Close-up view of the gate wire touching the EQR ring.

Gate wire was removed and re-probed. Unit completely recovered after removal of the gate wire. Damage on the passivation layer was evident after the gate wire was removed. (See Fig 7)

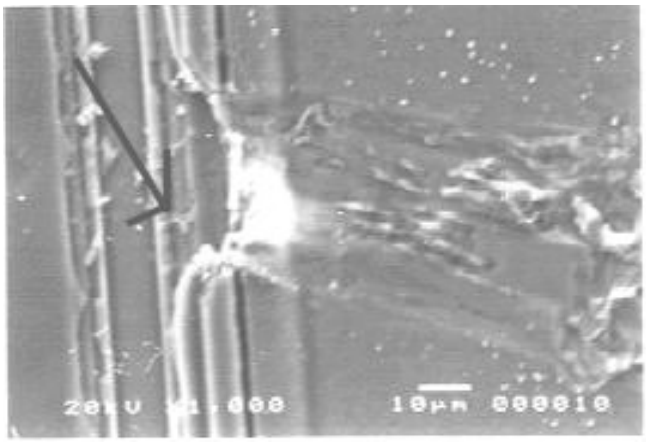


Figure 7. SEM photo of the passivation damage.

4.0 CONCLUSION

Root cause of the problem is definitely not product related UIL failures but the resistive path created by the gate wire and the EQR region by breaking the passivation layer.

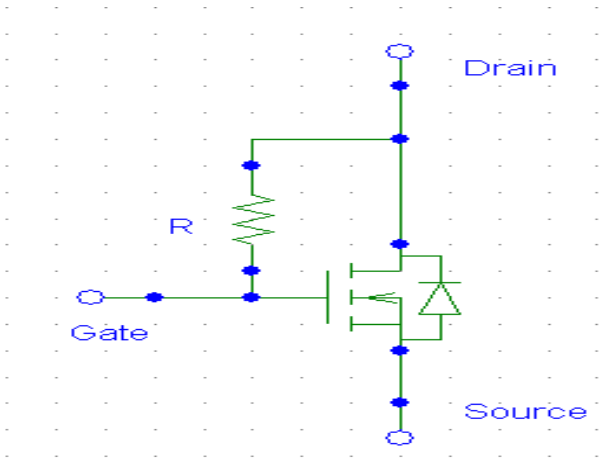


Figure 8. Failure model.

The resistance path created will appear across the gate and drain terminal since the EQR region is at drain potential. Data in experiment 2 showed that the failure mode is really BVdss. During the BVdss test, R will be across the drain and source terminals since the test is performed with the gate and source terminal tied together as the reference point or ground.

The failure model as shown in Fig. 8 also explains why the failures are screened by the BVdss test. A resistance path across D-S terminals will create a resistive breakdown curve.

Experiment 1 data also corroborate with the failure model. However, not all units with the same manifestation will fail UIL test since the value of R is not constant. Only those units that are close to zero resistance between gate and drain will fail UIL test. Those units that pass the UIL test will fail in the succeeding test (BVdss). This also explains why there are more BVdss failures in Split1-1 than Split1-2.

Therefore, the root cause of the higher percentage failure rate for UIL and BVdss at the subcontract facility is due to the breaking of the passivation layer by the gate wire.

5.0 RECOMMENDATIONS

Corrective actions made were to center the gate bond placement and revise the criteria for gate wire bonding. No portion of the gate wire was made to touch any area of the die except on the gate bond pad. This was done by replacing the bonding tool with a smaller wedge.

Die architecture and their function were also thoroughly discussed with process engineering.

6.0 ACKNOWLEDGMENT

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7.0 REFERENCES

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3. Ralph Locer, ***Introduction to Power MOSFETs and their Applications***, 1998.
4. Edgar Ancajas and Steven Sapp, ***EQR and the Metal Shorting Stripe***, 2000.

8.0 ABOUT THE AUTHOR

The author is a licensed Electronics and Communications Engineer. He earned his degree in 1995 from the University of San Carlos.

Joined Fairchild Semiconductor in February of 1996 (then National Semiconductor Corp) as a cadet product engineer for Analog products. Re-assigned to MOSFETs division also as a product engineer in February of 1997.

He has worked on majority of the packages for MOSFETs. Part of the team that launched the industry's first low voltage power MOSFET in a BGA package. Setup the first strip test system in Fairchild Semiconductor Cebu plant.