

EENG3106 Electronic Circuits Analysis I Laboratory

MOSFET I_D vs. V_{DS} Characteristics

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November 20, 2002
Revised December 1, 2004

Purpose:

This experiment has two aims.

1. Determination of the I_D vs. V_{DS} characteristics of the VN10LP n -channel enhancement-mode MOSFET;
2. Determination of the small-signal transconductance of the VN10LP under specified quiescent operating conditions.

Experimental procedure:

- 1). Connect the test circuit of Fig. 1. The VN10LP devices are prone to damage from electrostatic discharge (ESD); they should be left in the conductive foam until they are to be inserted in the circuit. Insertion of the VN10LP is to be the *last* step in construction of the test circuit.

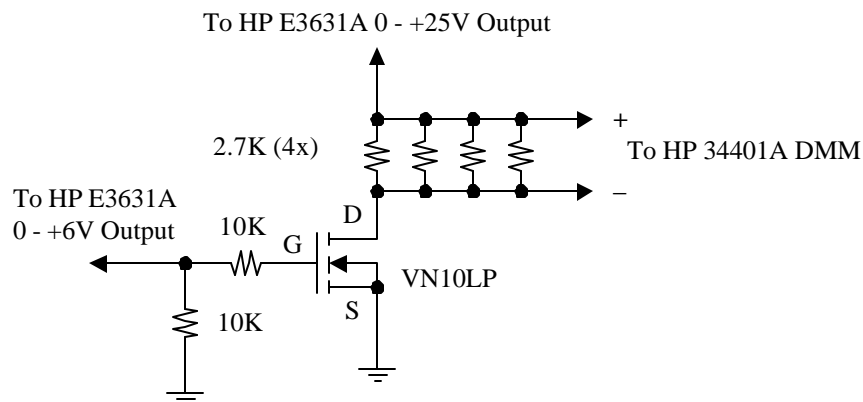


Figure 1. Test circuit for n -channel MOSFET I_D vs. V_{DS} characteristics. The source and substrate of the VN10LP are internally connected.

- 2). Boot the workstation and launch LabVIEW. Open the LabVIEW virtual instrument program BB_NMOS_V7F.vi.
- 3). Determine the threshold voltage $V_{GS(th)}$. For purposes of this experiment, the threshold voltage will be that which allows produces a drain current (I_D) in saturation of 20–30 μ A. (The MOSFET is in saturation when the gate-to-drain voltage V_{GD} is less than the threshold voltage. The drain current in saturation is essentially independent of drain-to-source voltage V_{DS}). Small values of drain current may be read from the digital readout of drain current on the lower left-hand of the virtual instrument screen or may be read from the I_D vs. V_{DS} display by temporarily changing the maximal drain current of the display from 30 mA to 0.5 mA. Note that the resolution of the digital readout is 10 μ A.
- 4). Use the virtual instrument to generate a series of I_D vs. V_{DS} curves with the gate-to-source voltage varied in steps of 0.2V starting at 0.2V above the threshold voltage until the maximal drain current approaches full scale of the display. See Fig. 2 for an example. (Repeat this step with steps of 0.1V starting at 0.1V above threshold if an I_D vs. V_{DS} display with at least four distinct curves is not obtained).

5). Measure the transconductance of the MOSFET at $I_D = 5\text{mA}$ and 10mA at $V_{DS} = 10\text{V}$. This may be accomplished by first determining experimentally the V_{GS} required to cause the I_D vs. V_{DS} curve to pass through the specified (I_D, V_{DS}) point and subsequently dithering V_{GS} about this experimental value. Transconductance may be estimated as the ratio $\Delta I_D / \Delta V_{GS}$.

Results to be reported:

- 1). Report the measured threshold voltage.
- 2). Show the I_D vs. V_{DS} characteristics.
- 3). Report the transconductance values.

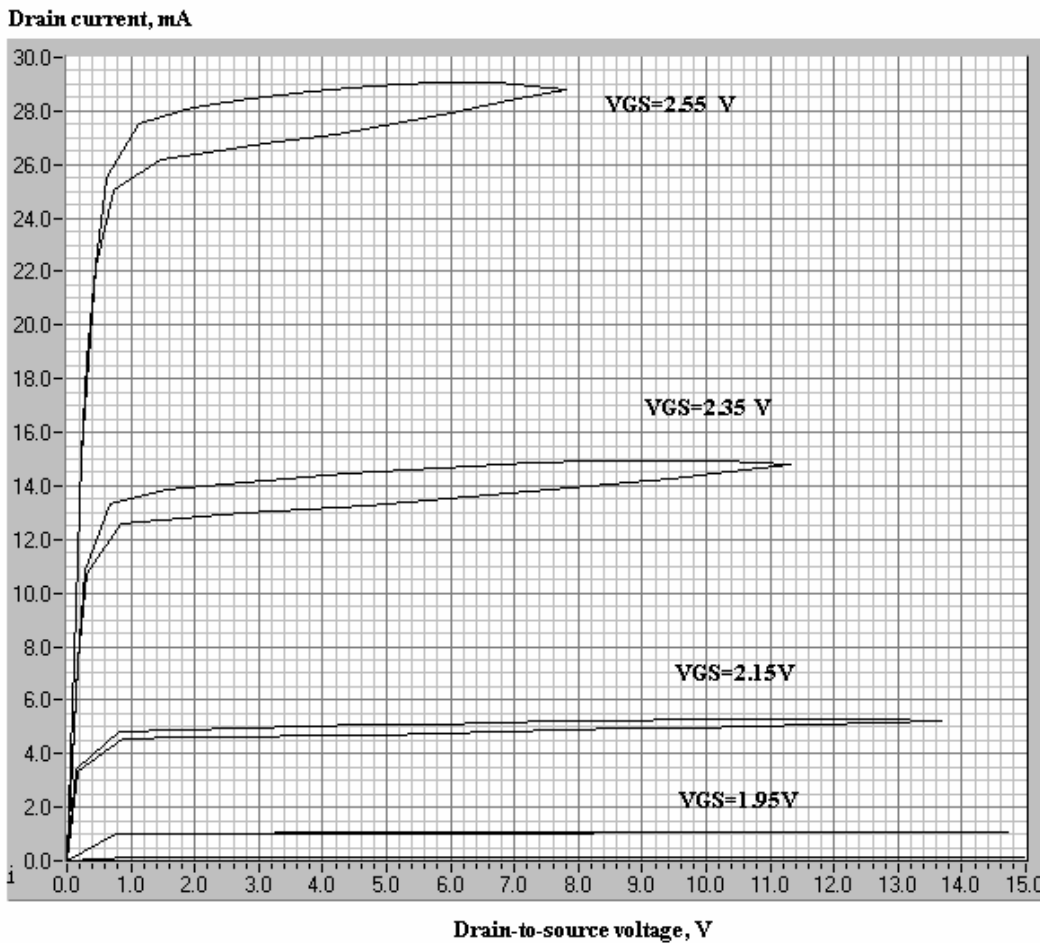


Fig. 2. Screen image of the I_D vs. V_{DS} characteristics of a VN10LP MOSFET acquired with Labview virtual instrument program BB_NMOS.vi (predecessor to the virtual-instrument program used in this experiment). The threshold voltage of this particular device was found to be 1.55V; curves were taken with V_{GS} increments of 0.2V beginning at $V_{GS}=1.75\text{V}$. The I_D vs. V_{DS} curve for $V_{GS}=1.75\text{V}$ lies just above the abscissa and is not labeled due to lack of space.