BOISE STATE UNIVERSITY

## *DoD MURI – Program Review*

# Degradation in gate dielectrics and the effects on simple integrated circuit building blocks (SICBBs)

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College of Engineering

# Acknowledgments


- University Involvement

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# MURI Supported Journal & Conference Publications

## (*denotes student authors)


- Southwick III*, Richard G. and William B. Knowlton, *Stacked Dual Oxide MOS Energy Band Diagram Visual Representation Program*, IEEE Transactions on Device and Materials Reliability, (2006) - accepted for publication.
- T. L. Gorseth*, D. Estrada*, J. Kiepert*, M. L. Ogas*, B. J. Cheek*, P.M. Price, R. J. Baker, G. Bersuker, W.B. Knowlton, *Preliminary Study of NOR Digital Response to Single pMOSFET Dielectric Degradation*, presented at the Workshop on Microelectronic Devices (Boise, Idaho; April 14, 2006)
- M. L. Ogas*, P. M. Price*, J. Kiepert*, R. J. Baker, G. Bersuker, and W. B. Knowlton, *Degradation of Rise Time in NAND Gates Using 2.0 nm Gate Dielectrics*, oral presentation and publication at the 2005 IEEE Integrated Reliability Workshop, (October 2005) p. 63-66.
- Ogas* M. L., R. G. Southwick III* B. J. Cheek* R. J. Baker, G. Bersuker, W. B. Knowlton, *Survey of Oxide Degradation in Inverter Circuits Using 2.0nm MOS Devices*, in proceedings of the 2004 IEEE International Integrated Reliability Workshop, (Oct. 2004), pp. 32-36.
- Cheek* Betsy J., Stutzke* Nate, Santosh Kumar, R. Jacob Baker, Amy J. Moll and William B. Knowlton, *Investigation of Circuit-Level Oxide Degradation and its Effect on CMOS Inverter Operation Performance and MOSFET Characteristics*, in proceedings of the 2004 IEEE International Reliability Physics Symposium (April, 25-29, 2004) pp. 110-116.
- Kumar, Santosh, William B. Knowlton, Sridhar Kasichainula and Cesar Payan, *SRAM Subthreshold Current Recovery after unipolar AC stressing*, in proceedings of the 2004 IEEE International Reliability Physics Symposium (April, 25-29, 2004) pp. 46-48.
- Stutzke*, N., B.J. Cheek*, S. Kumar, R.J. Baker, A.J. Moll and W.B. Knowlton, *Effects of Circuit-Level Stress on Inverter Performance and MOSFET Characteristics*, in proceedings 2003 IEEE International Integrated Reliability Workshop, (Oct, 20-23, 2003) pp. 71-79.
- Payan, C., S. Kumar, A. Thupil, S. Kasichainula and W.B. Knowlton, *Leakage Current Recovery in SRAM after AC stressing*, in proceedings 2003 IEEE International Integrated Reliability Workshop, (Oct, 20-23, 2003) pp. 67-70.
- Lawrence*, C.E., B.J. Cheek*, T.E. Lawrence*, Santosh Kumar, A. Haggag, R.J. Baker, and W.B. Knowlton, *Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach*, in Proceedings of the 15th Biennial IEEE University/Government/Industry Microelectronics (UGIM) Symposium, June 30 - July 2, 2003, pp.263-266.
- Kumar, Santosh and William B. Knowlton, *Alternate method of TDDB study for aluminum oxide using magneto-resistance*. in IEEE International Integrated Reliability Workshop, (2002) pp. 180-183.
- Knowlton, W.B., T. Caldwell*, J.J. Gomez*, and S. Kumar. *On the nature of ultrathin gate oxide degradation during pulse stressing of nMOSCAPs in accumulation*. in IEEE International Integrated Reliability Workshop, (2001) pp. 87-88.

# MURI Supported Conference Presentations, Posters and Extended Abstracts (to show inclusion of UG and Grad students as authors*)

- Richard Southwick III*, Michael Ogas* and William B. Knowlton, *Interactive dual oxide MOS energy band diagram program*, poster presentation at the 2005 IEEE International Integrated Reliability Workshop, (October 2005).
- Richard G. Southwick III*, Vaughn Johnson*, Joe Lindsey*, Tim Lawrence*, Jim Jozwiak, Amy Moll, William B. Knowlton, *Through Wafer Interconnects: Preliminary Investigation Of Plasma Induced Damage In pMOSFETs By BOSCH DRIE*, poster presentation at 2004 IEEE International Integrated Reliability Workshop, (Oct. 2004).
- Ogas*, Michael, Richard Southwick III*, Betsy Cheek*, Carrie Lawrence*, BSU, Santosh Kumar, Amr Haggag, Jacob Baker, and William Knowlton, *Multiple Waveform Pulse Voltage Stress Technique for Modeling Noise in Ultra Thin Oxides,* poster presentation at Workshop on Microelectronics and Electron Devices, (Boise, Idaho, April 16, 2004).
- Ogas, Michael*, Dorian Kiri*, Ouahid Salhi*, Richard Southwick III*, Betsy Cheek*, William B. Knowlton, *Investigation of Ultra Thin Gate Oxide Reliability in MOS Devices and Simple ICs*, poster presentation at Workshop on Microelectronics and Electron Devices, (Boise, Idaho, April 16, 2004) and at 2004 IEEE International Integrated Reliability Workshop, (Oct. 2004).
- Ogas*, M. L., R. G. Southwick III, B. J. Cheek*, C. E. Lawrence*, S. Kumar, A. Haggag, R. J. Baker, W. B. Knowlton, *Investigation of Multiple waveform pulse voltage stress (MWPVS) technique in ultrathin oxides*, poster presentation at the 2003 IEEE International Integrated Reliability Workshop (Oct, 20-23, 2003).
- Stutzke*, Nate, Betsy J. Cheek*, and William B. Knowlton, *Circuit-level stress and gate dielectric degradation in MOSFETs*, oral presentation and poster at the 2003 Micron Foundation Summer Technical Conference, Boise, ID (August 8, 2003). [Awarded Best Poster Award]
- Southwick III, R.G. *, Betsy Cheek* and William B. Knowlton, *Charge pumping techniques for MOS devices*, oral presentation and poster at the 2003 Micron Foundation Summer Technical Conference, Boise, ID (August 8, 2003).
- Cheek, Betsy*, Carrie Lawrence*, Tim Lawrence*, Jose Gomez*, Theodora Caldwell*, Dorian Kiri*, Santosh Kumar, Jake Baker, Amy J. Moll and William B. Knowlton, *Gate dielectric degradation effects on nMOS devices and simple IC building blocks (SICBBs)*, extended abstract accepted for poster session at IEEE/EDS Workshop on Microelectronics and Electron Devices, (October 25, 2002).
- Lawrence*, C., B. Cheek*, T. Caldwell*, T. Lawrence*, D. Kiri*, S. Kumar, J. Baker, A. J. Moll and W. B. Knowlton, *Pulse voltage stressing of ultrathin gate oxides in NMOS devices*, poster session at the IEEE International Integrated Reliability Workshop, (October 21-24, 2002).
- Cheek*, B., C. Lawrence, T. Lawrence*, T. Caldwell*, D. Kiri*, S. Kumar, J. Baker, A. J. Moll and W. B. Knowlton, *Circuit level reliability of ultrathin gate oxides for SICBBs: Preliminary study concentrated on the effect of stress on the NMOSFET of an inverter*, poster session at the IEEE International Integrated Reliability Workshop, (October 21-24, 2002).
- Knowlton, William B., *Research efforts in materials science related areas at Boise State University*, invited talk at Idaho State University-Idaho Accelerator Center Workshop on "Application of Novel X-ray sources to Biological and Materials Science" (September 5 & 6, 2002).

# Outline

- Statement of Work for Gate Oxide Reliability
- Measurement Techniques Developed
- Circuits Studied Relative to Gate Oxide Thickness
- Alternative Gate Dielectrics
- Future Work

# Statement of Work

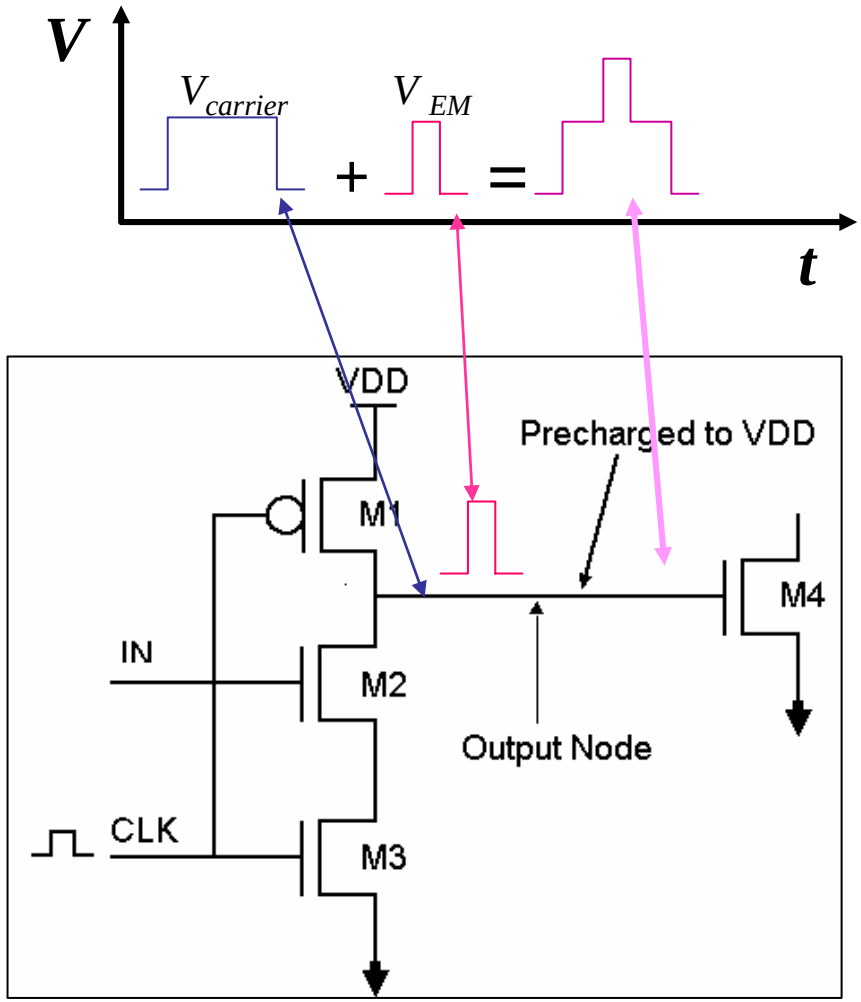
- **Focus**: Gate dielectric/oxide ($SiO_2$) degradation by EM radiation in MOSFETs & Effects on ICs
  - Determine degradation mechanisms in gate dielectric due to EM radiation
  - Mimic EM radiation-induced degradation in gate oxides using DC techniques
  - Determine how gate oxide degradation mechanisms affect simple integrated circuit building blocks
    - ✓Inverters
    - ✓Logic gates: NAND & NOR
- To do this: Developed 2 - test and measurement techniques
  - ***1) Multi-Waveform Pulse Voltage Stressing***
  - ***2) Switch Matrix Technique***

# Techniques for Examining EM Radiation Effects on Devices and Circuits

- ***Multi-Waveform Pulse Voltage Stressing (MWPVS)***
- ***Switch Matrix Technique***

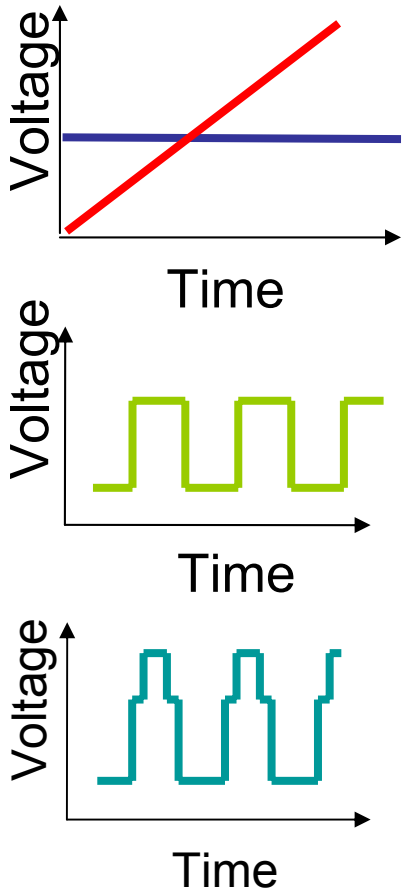
# Multi-waveform Pulse Voltage Stressing (MWPVS)
## - Mimics EM Radiation-IC Coupling

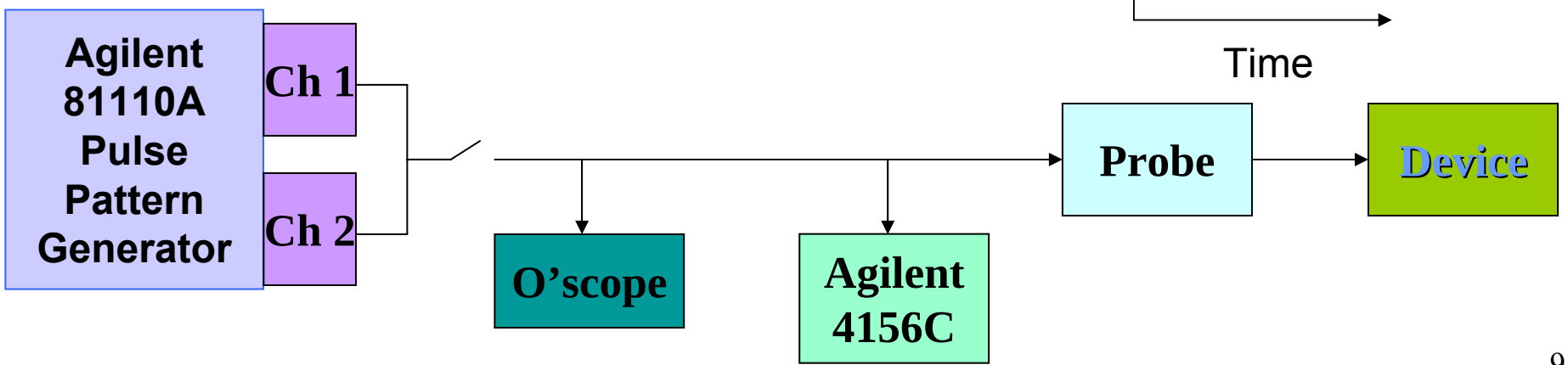
- Continued size reduction in ICs, leads to:
  - Very close interconnect proximity
  - EM radiation will Capacitive Couple to Interconnects
  - Cause noise spiking
  - Increase voltage:
    - ✓From: $V_{carrier}$
    - ✓To: $V_{carrier} + V_{EM} = V_{noise}$



# Reliability Test Methods

- RVS (ramped voltage stress)
  - DC – difficult to extract time dependency
- CVS (constant voltage stress)
  - DC - NOT typical for digital circuit operation
- PVS (pulse voltage stress)
  - Better mimics digital device behavior
- **MWPVS**
  - Represents circuit operation with noise source such as EM radiation

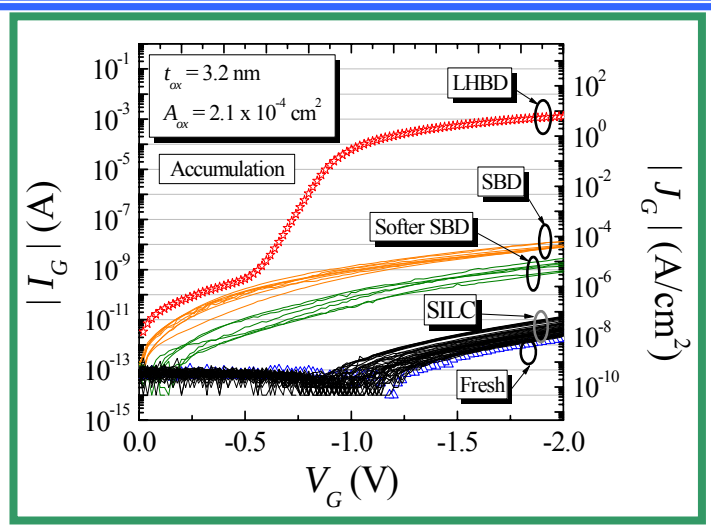


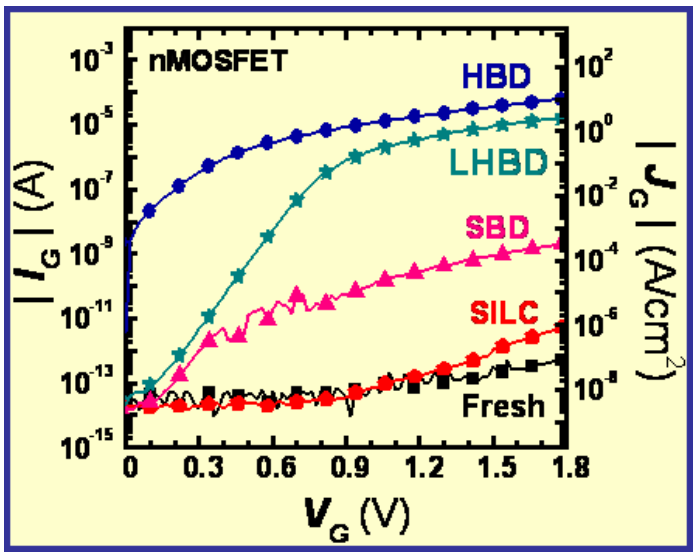
# MWPVS - Experimental Results

- Pre- and post- MWPVS $I_{GATE}$-$V_{GATE}$ results:
  - Degradation mechanisms observed
    - ✓ SILC (Stress Induced Leakage Current)
    - ✓ SBD and Softer SBD (Soft Breakdown)
    - ✓ LHBD (Limited Hard Breakdown)
    - ✓ HBD (Hard Breakdown)

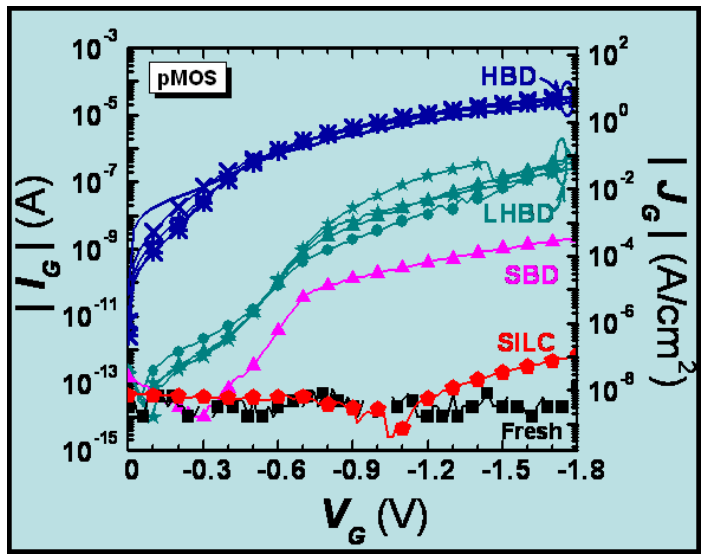
MWPVS




CVS




CVS

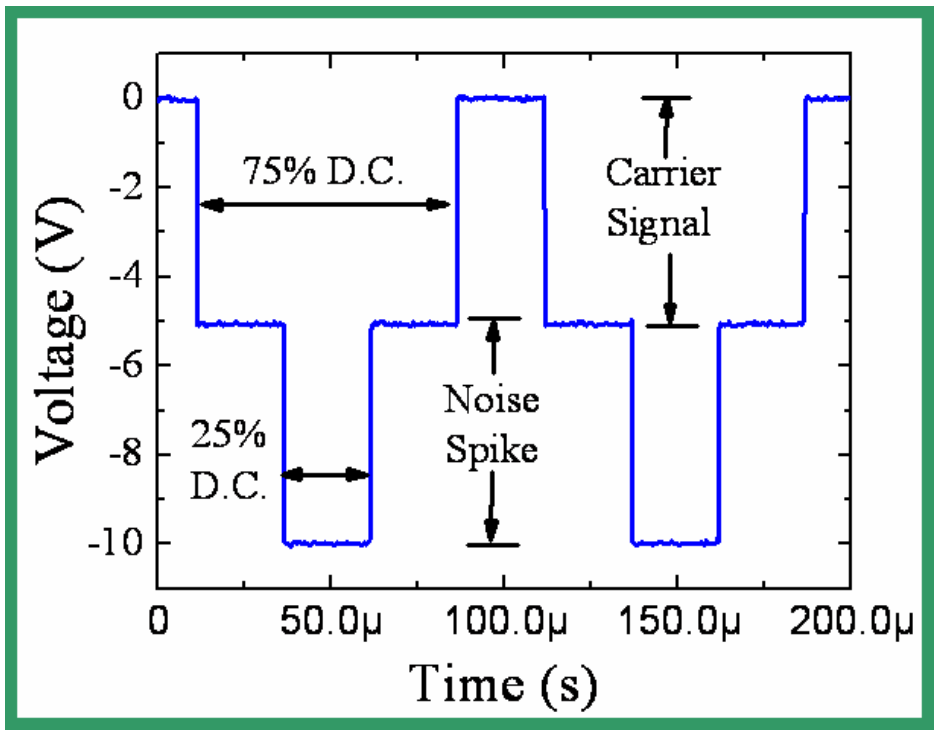



**Finding**: Degradation mechanisms induced by either EM-like pulse voltage stressing or DC stress the same.

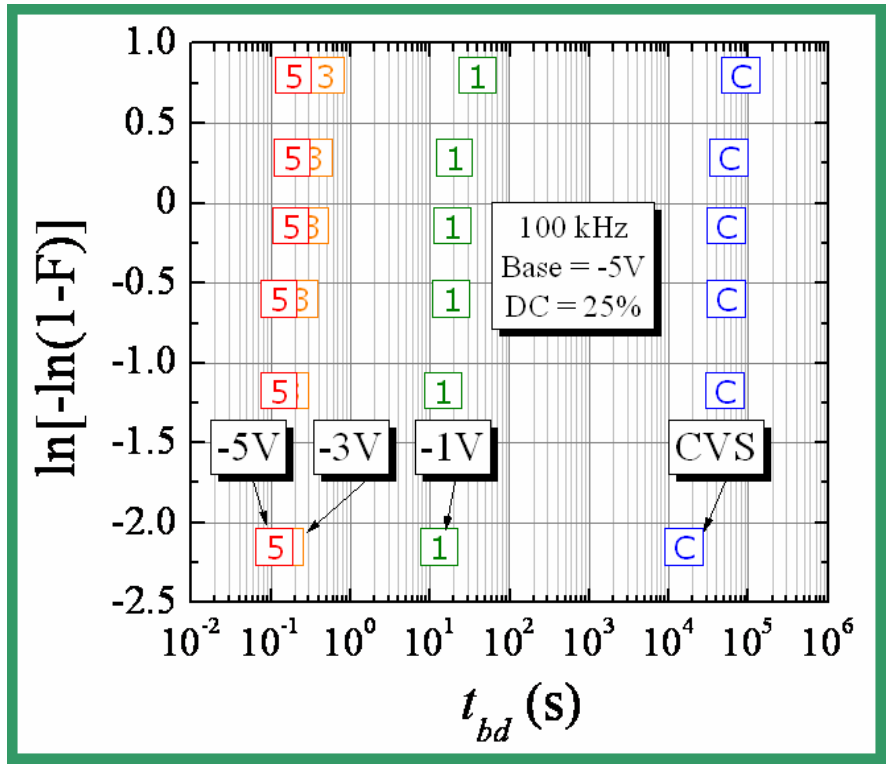
# MWPVS vs CVS

- *Weibull plots* indicate device lifetime decreases by orders of magnitudes when compared to preliminary CVS data

MWPVS



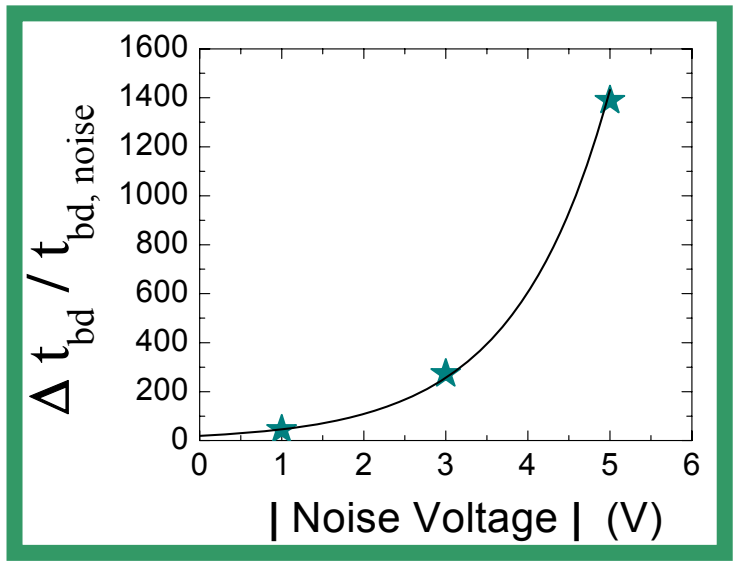

Weibull Plots




Similar results for lower frequencies

# Preliminary Noise Model for MWPVS

- Initial data indicates that increasing the noise signal decreases device lifetime exponentially†
  - *d*, constant proportional to $DC_{BASE}$ of carrier signal
  - *d'*, constant proportional to $DC_{SPIKE}$ of noise signal
  - *c*, voltage accelerator factor
  - *dV*, noise amplitude




$$\frac{1}{t_{bd,noise}} \approx d \cdot e^{c|V|} + d' \cdot e^{c(|V|+|dV|)}$$

Preliminary noise model for a spike voltage with a $DC_{SPIKE}$ of 20%

EM Radiation can cause significant reduction in lifetime (over 3 orders of magnitude)

$$\Delta t_{bd} = \frac{t_{bd} - t_{bd,noise}}{t_{bd,noise}}$$

$$t_{bd} = T \cdot DC_{BASE} \cdot P_{bd}$$

†Lawrence, C.E., et al, "Gate Dielectric Degradation Effects on nMOS Devices Using a Noise Model Approach", in Proc. of the 15th Biennial IEEE UGIM Symposium, June 30 - July 2, 2003, pp.263-266.

# Conclusions

- Designed a MWPVS technique to simulate effects of EM radiation on MOSFETs
- Reliability Issues
  - ✓Constructive Interference occurs due Superposition of waveforms
    - o Electromagnetic radiation
    - o Capacitive Coupling
    - o Mixed Signals
- Device lifetime shorter for EM-like radiation than PVS or CVS

**Data corresponds to the noise model**: Device lifetime exponentially decreases with increase in noise voltage

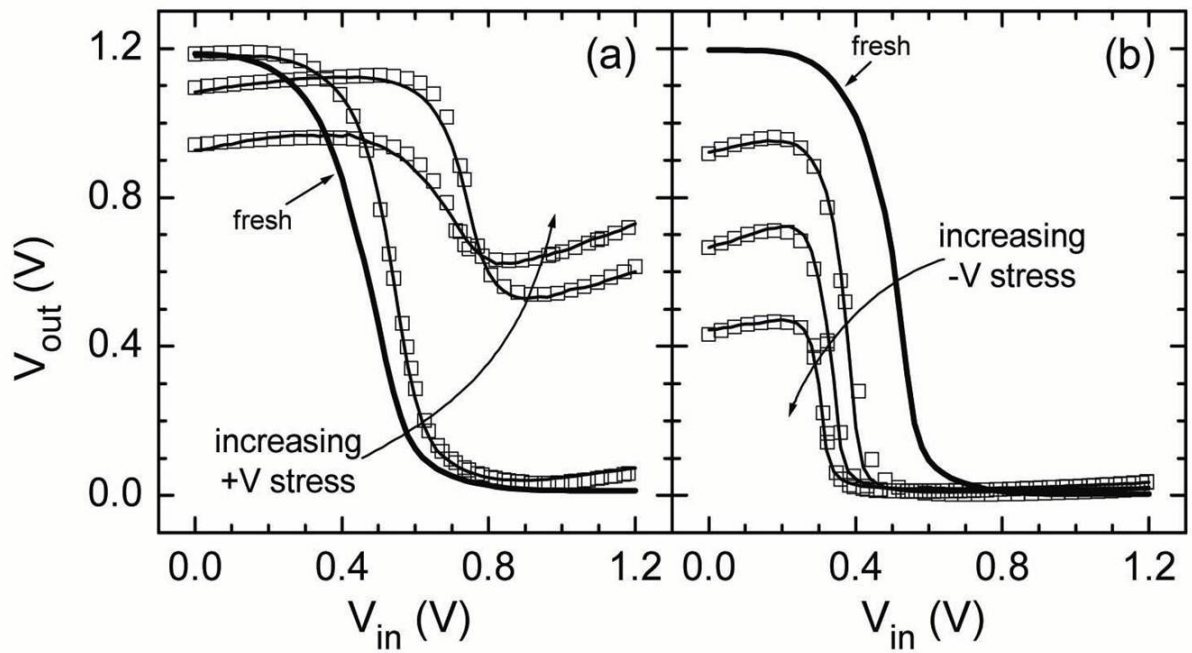
# Techniques for Examining EM Radiation Effects on Devices and Circuits

- ***Multi-Waveform Pulse Voltage Stressing (MWPVS)***
- ***Switch Matrix Technique (SMT)***

# Gate Oxide Reliability in Simple IC Building Blocks (SICBBs)

- Only one other group examining SICBB reliability
- They can only perform VTC – a DC technique

Inverter




- They did not examine time domain
- Cannot determine oxide degradation mechanism
- Why? Because they cannot examine *individual* MOSFETS

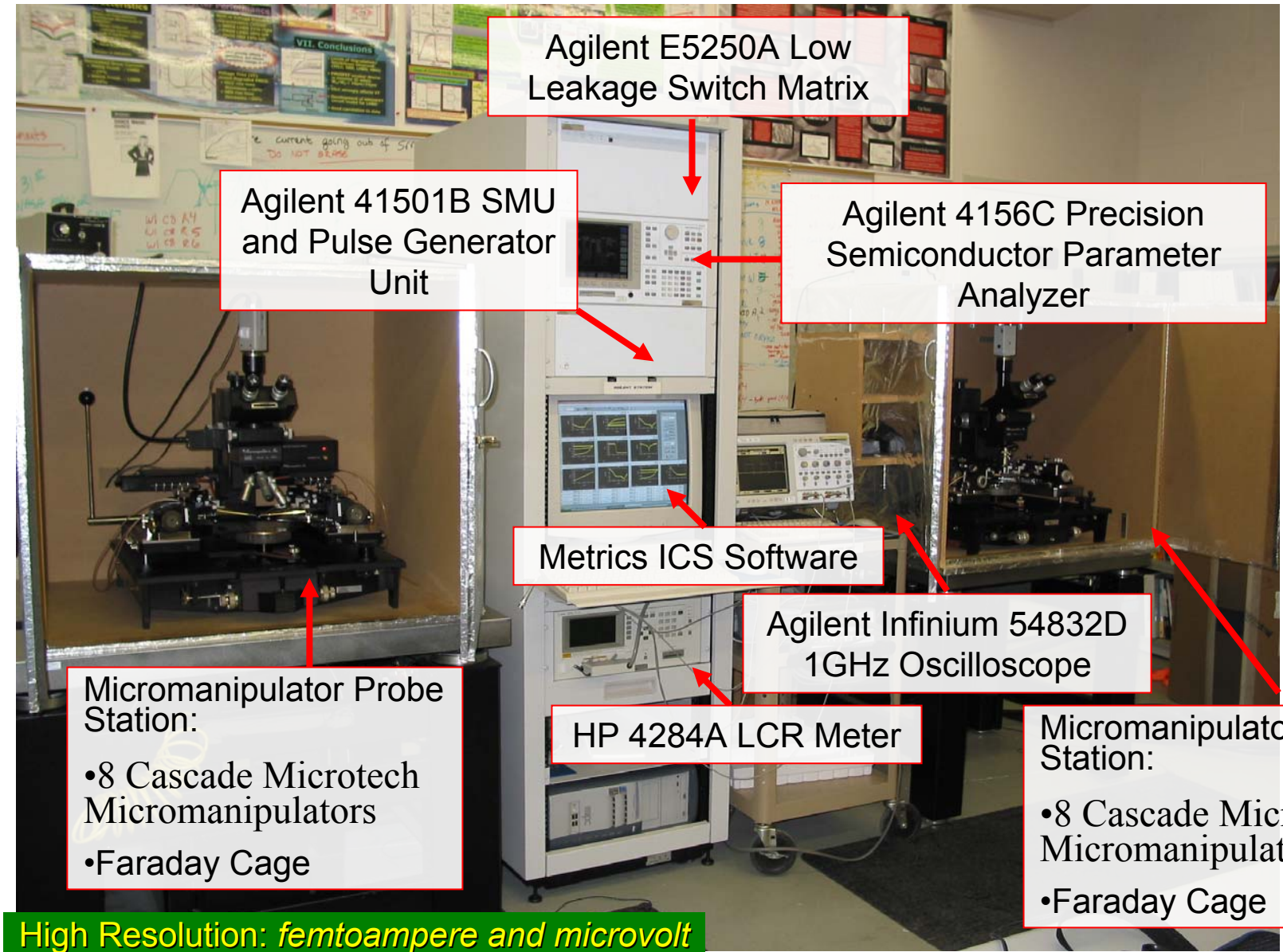
[1] J.H. Stathis, R. Rodriguez, B.P. Linder, "Circuit Implications of Gate Oxide Breakdown," *Proceedings WoDIM*, 2002.

# Switch Matrix Technique (SMT)

- Reliability studies - focus mainly on MOSFETS and large-scale ICs.
- Degradation effects in MOSFETs cannot be directly correlated to gate oxide degradation in ICs
- **ANSWER**: We developed a method that can isolate MOSFET from IC to:
  - examine EM-radiation-like oxide degradation in individual MOSFETs
  - Induce EM-radiation-like oxide degradation in individual MOSFETs or circuit
- **METHOD**: Switch Matrix Technique (SMT) enables reliability studies at the **simple integrated circuit building block (SICBB)** level.[1]
- Using SMT, reliability studies have focused on the following **SICBBs**:[1,2]
  - Inverter ($t_{ox}$: 3.2 and 2 nm)
  - Transmission Gate (TG not shown)
  - NAND ($t_{ox}$: 2 nm)
  - NOR ($t_{ox}$: 2 nm)

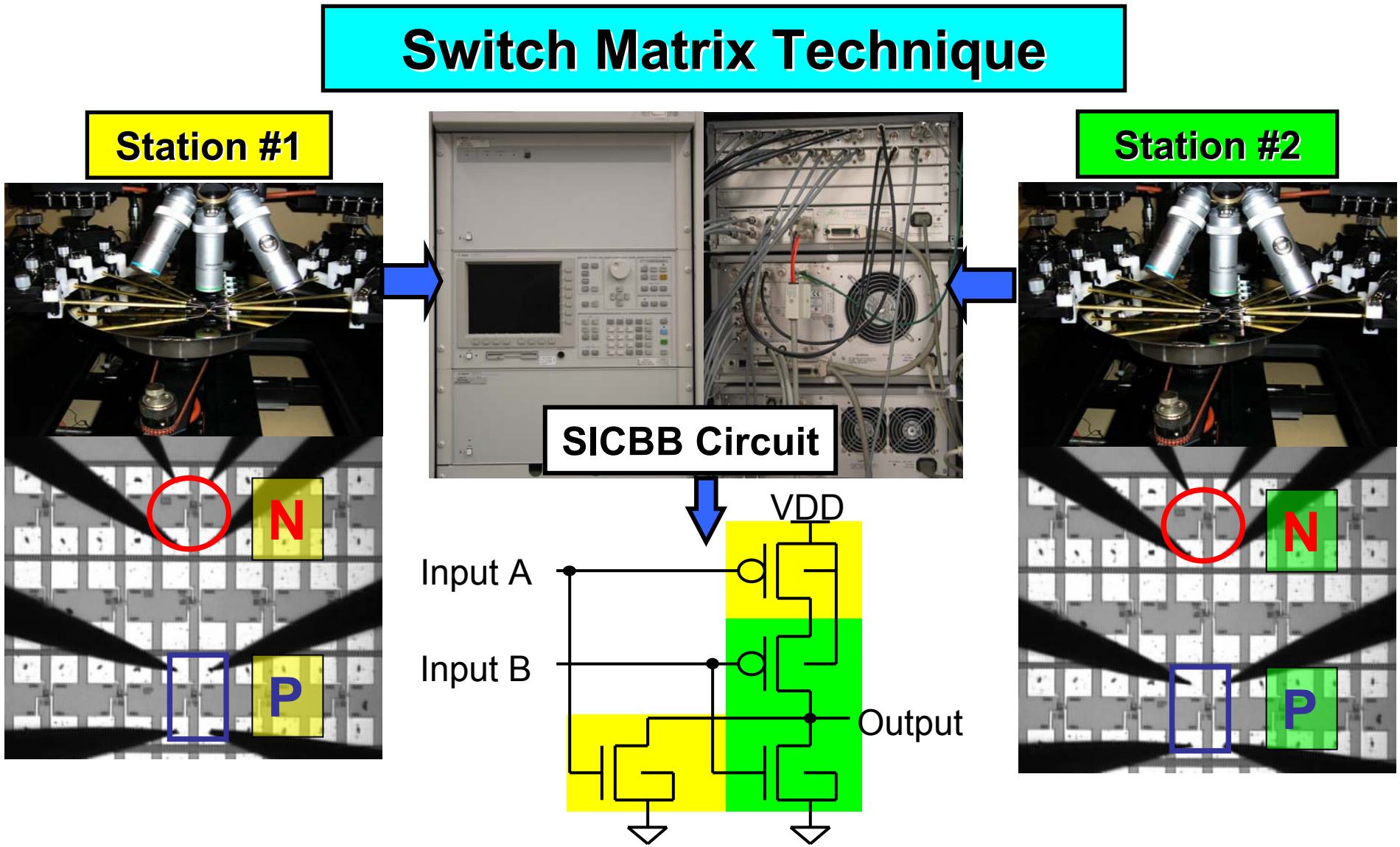
[1]B. Cheek, *et al.*, "Investigation of circuit-level oxide degradation and its effect on CMOS inverter operation and MOSFET characteristics," in *2004 Proc. IEEE IRPS*, pp. 110-116.
[2]M. L. Ogas, *et al.*, "Degradation of risetime in NAND gates using 2nm gate dielectrics," in *2005 Proc. IEEE IIRW*, pp. 63-66.

# Switch Matrix Technique (SMT) - System



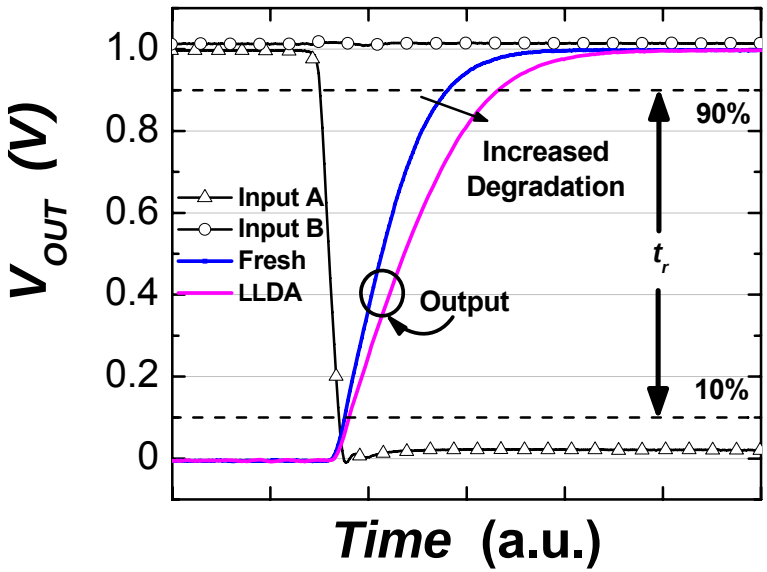

High Resolution: *femtoampere and microvolt*

# Switch Matrix Technique (SMT) - Experimental Setup

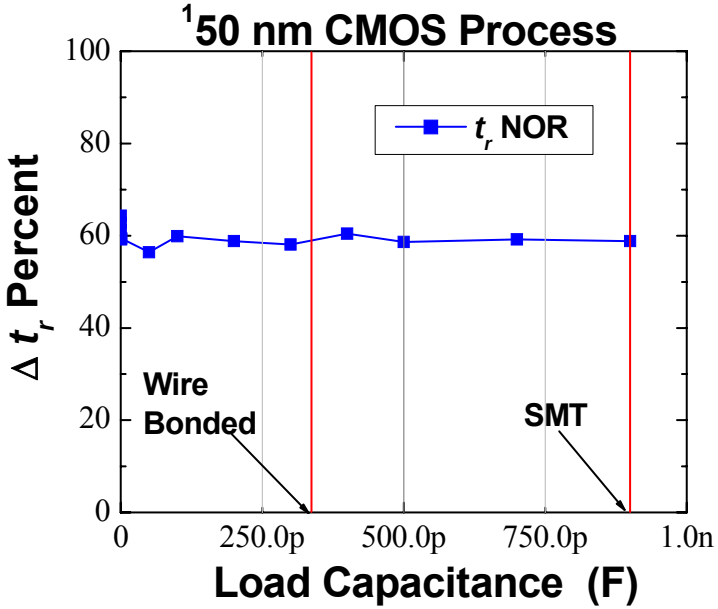


# Switch Matrix Technique (SMT) - Addressing Load Capacitance

## Experimental




## Simulation



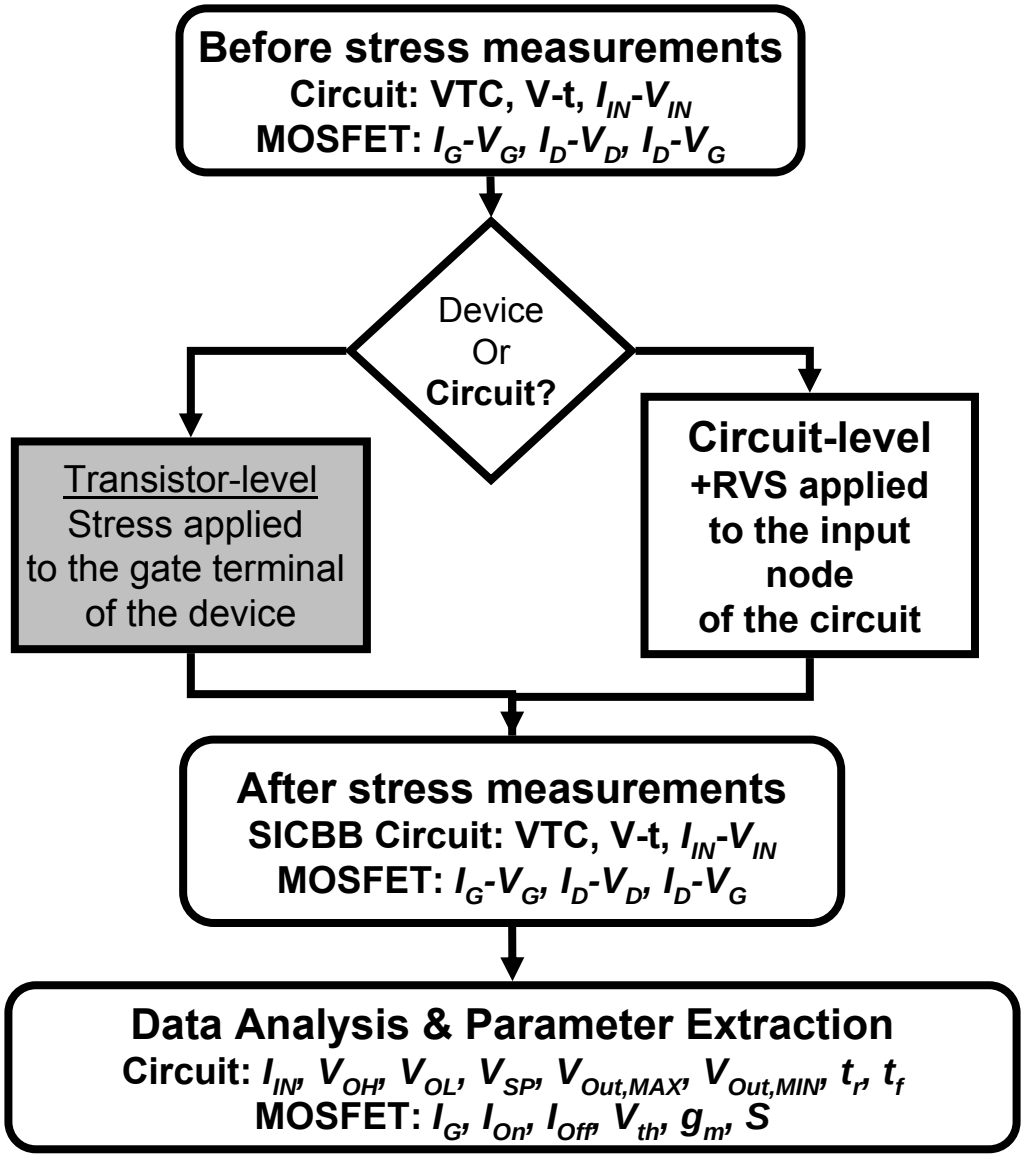

$\Delta t_r$ is within standard deviation when comparing wire bonded NAND circuit and SMT NAND circuit.

Simulation of NOR circuit shows when $C_{load}$ is decreased, $\Delta t_r$ percent remains constant.

**SMT is a viable technique**

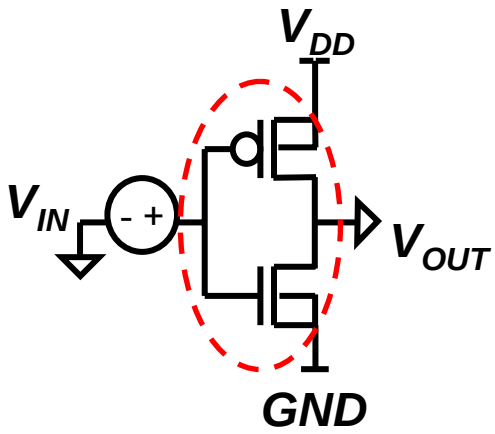
[1]R. J. Baker, "CMOS: Circuit design, layout, and simulation," 2 ed: IEEE Press Wiley-Interscience, 2005, pp 278, 154-158.

# SMT Experimental Procedure

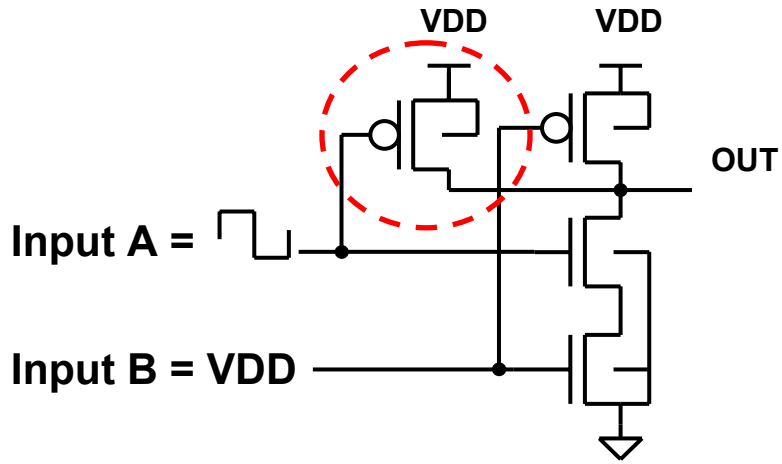


# SMT – SICBBs Studied

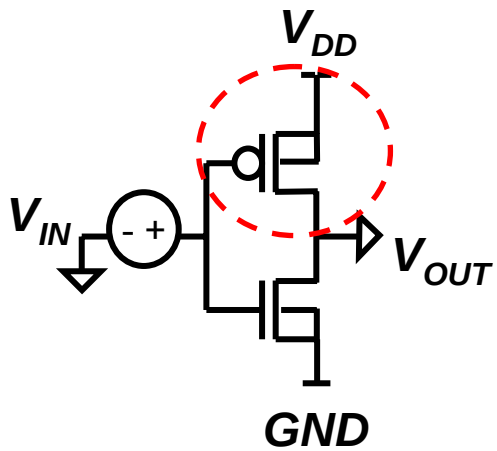
**SICBB: 3.2nm Inverter**
**Circuit Level Degradation**



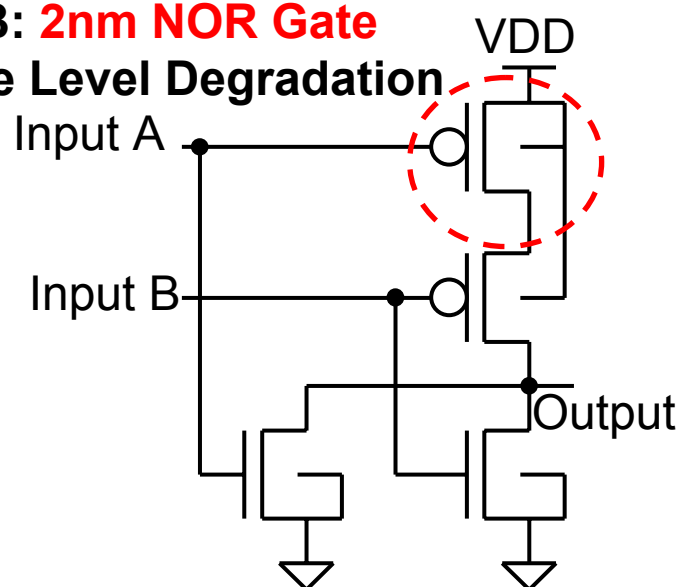

**SICBB: 2nm NAND Gate**
**Device Level Degradation**



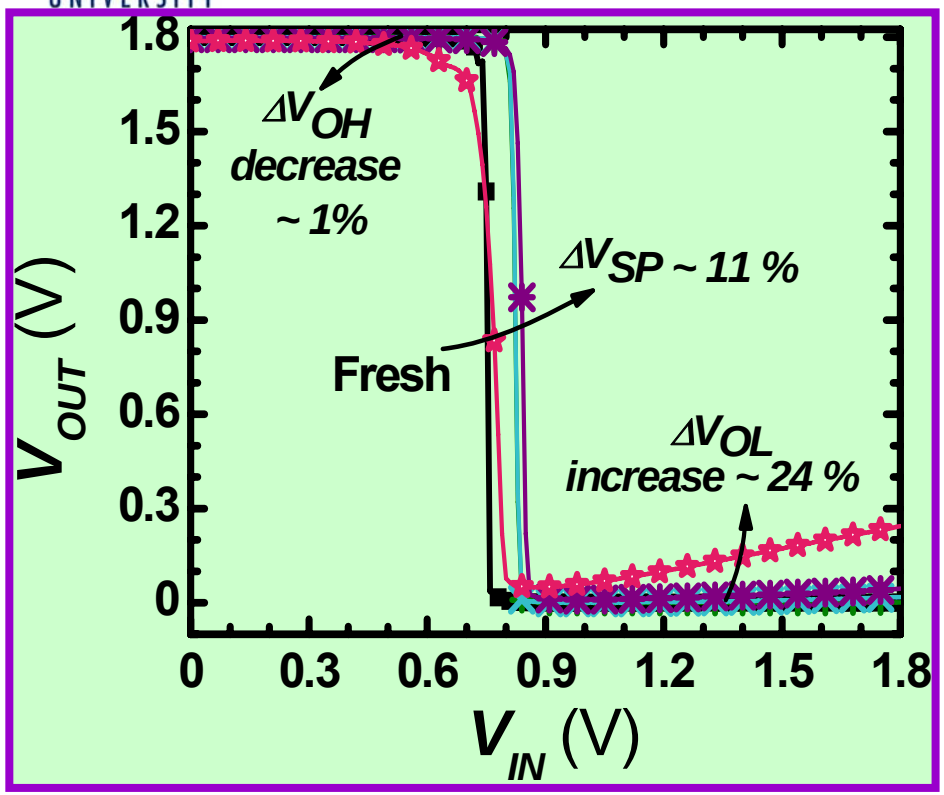

**SICBB: 2nm Inverter**
**Device Level Degradation**




**SICBB: 2nm NOR Gate**
**Device Level Degradation**

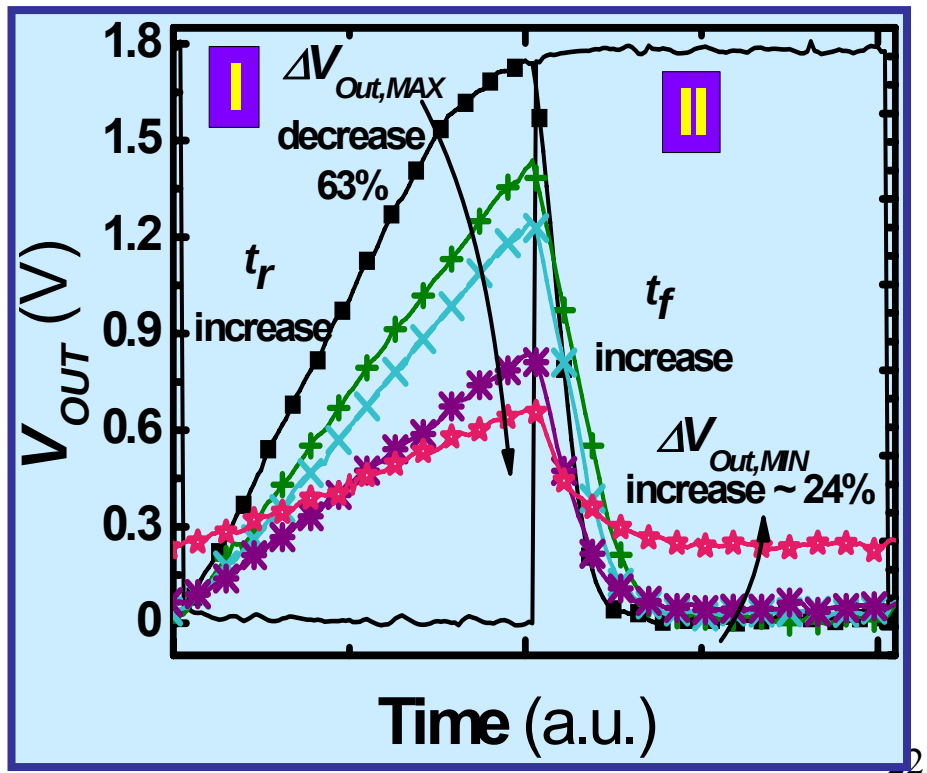


# 3.2nm Inverter VTC and V-t Response



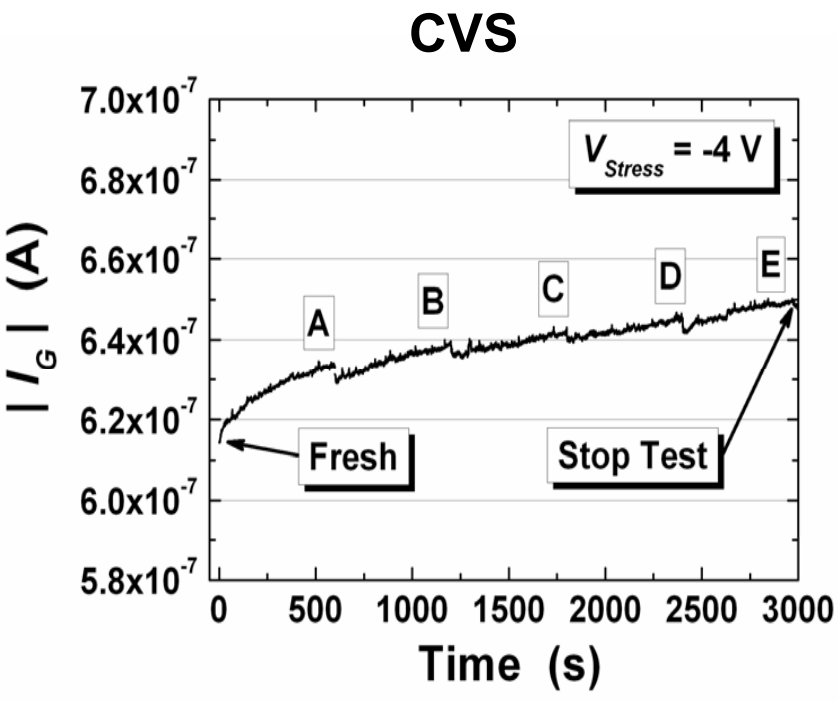

**Increasing Degradation**

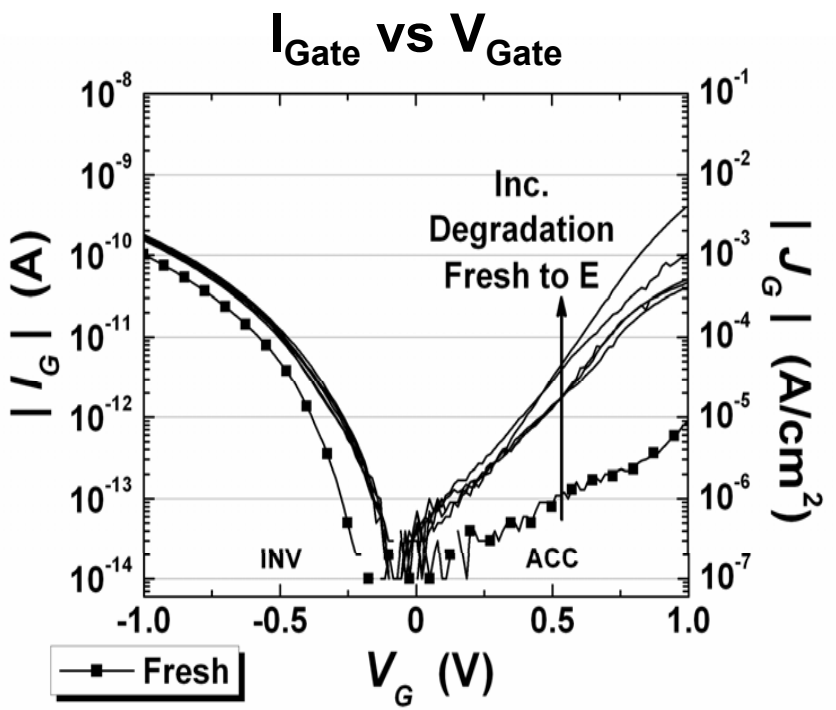
- Fresh
- LHBD (*P*,*N* )
- LHBD (*P*,*N* )
- HBD (*P*), *LHBD* (*N*)
- HBD (*P*,*N*)




- **Time-domain degradation more significant!**
  - $\Delta V_{OH} << \Delta V_{Out,MAX}$
  - $\Delta V_{OL} = \Delta V_{Out,MIN}$

# 2nm pMOSFET Gate Oxide Degradation ($I_G$-$V_G$)

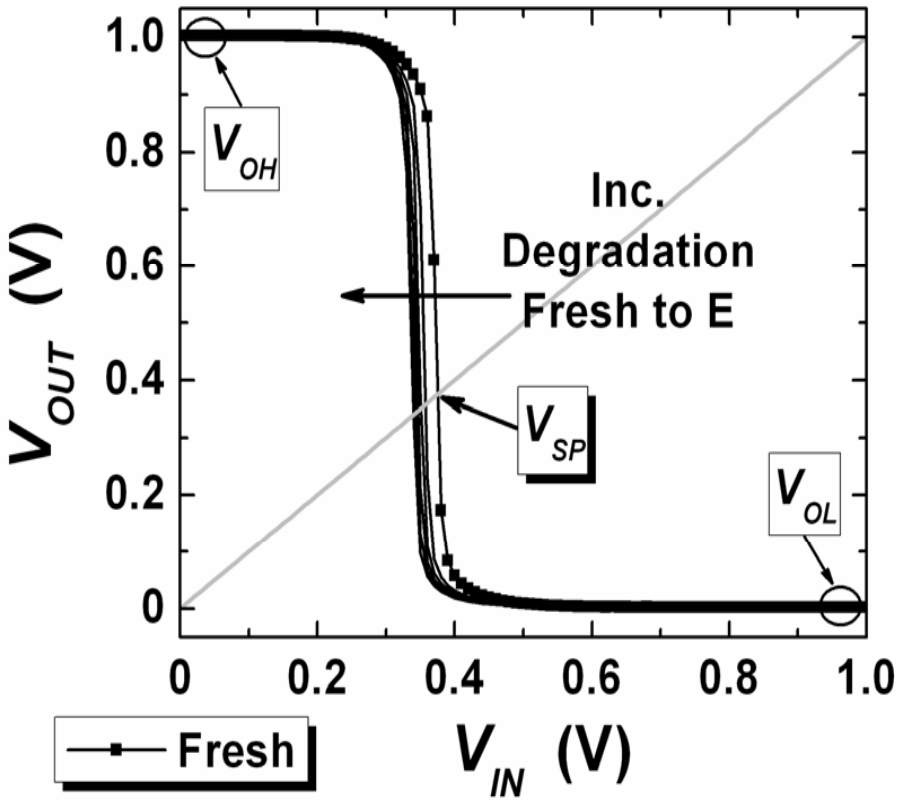


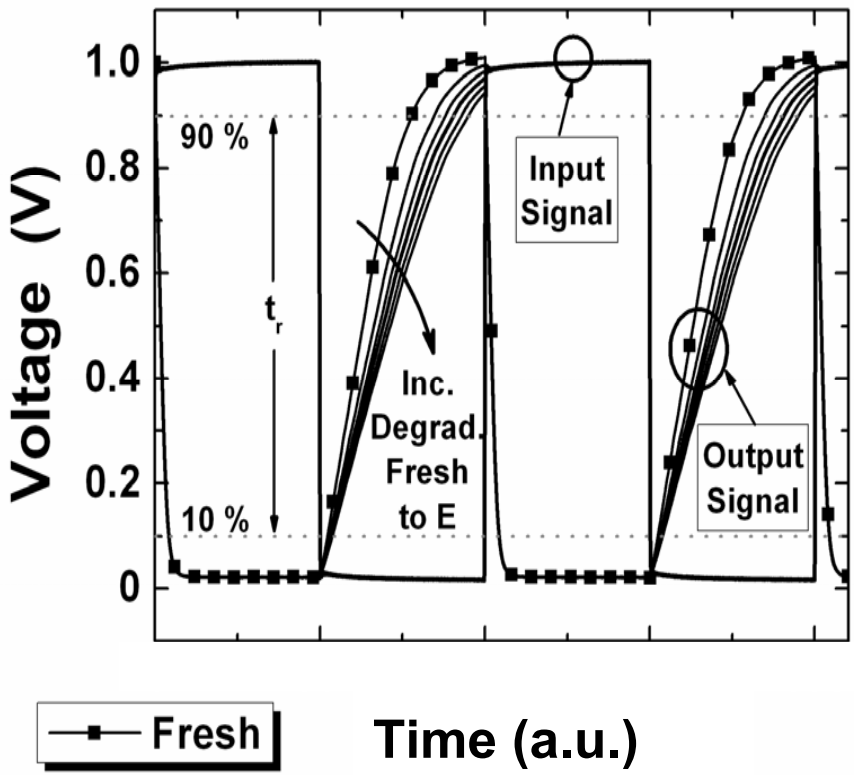

- Observed gate leakage current increase (2.0 nm)
  - Accumulation mode ~ 2 to 3 orders of magnitude
  - Inversion mode < 1 order of magnitude

# 2nm Inverter VTC and V-t Response

## DC Operation




## AC Operation




Fresh → E level degradation:

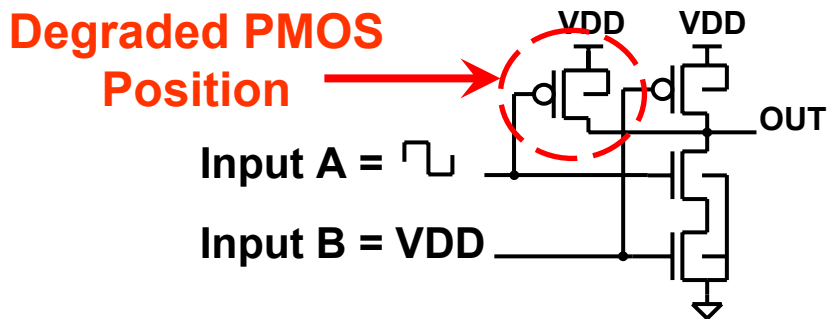
- Δ $V_{SP}$ ~8% shift left[1]
- Output behavior transitions from 1 to 0

Fresh → E level degradation

Δ rise time[1] ~36% to 62%

[1]R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS: Circuit design, layout, and simulation," IEEE Press, pp. 201-228, 1998.

# 2nm NAND Gate VTC and V-t Response

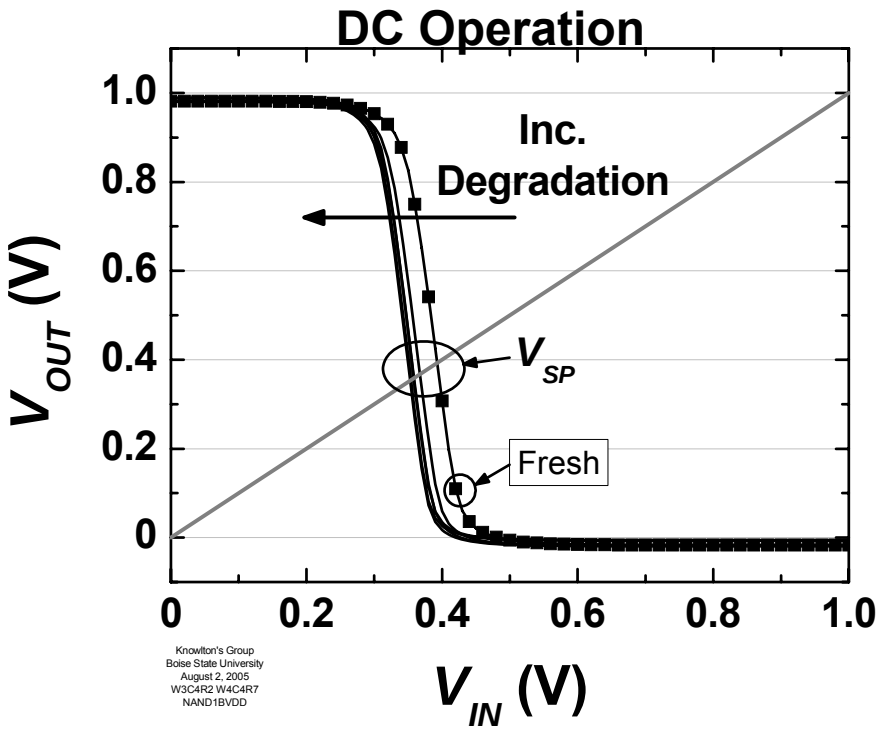


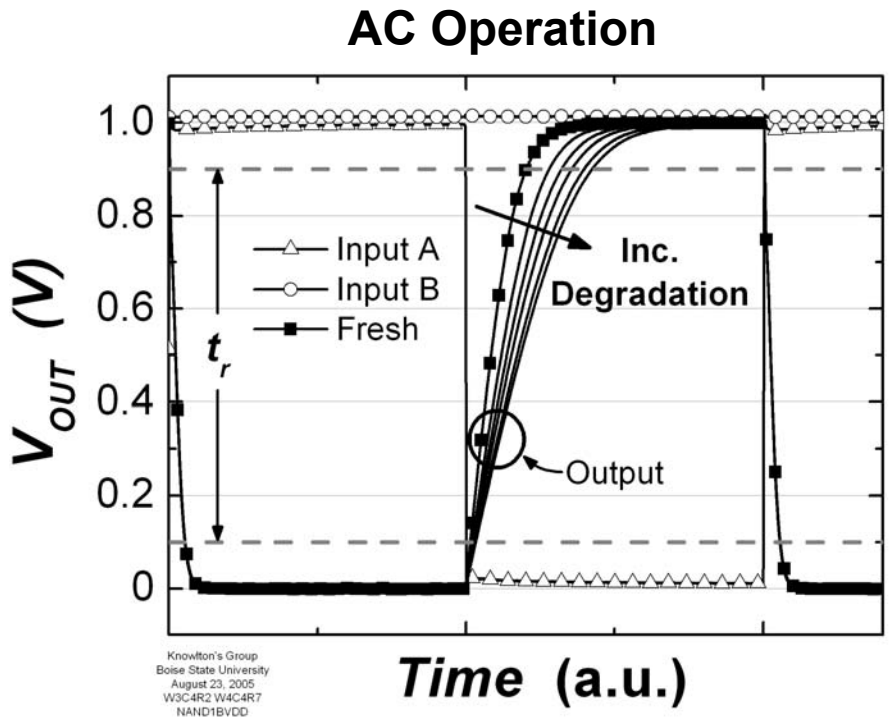

$\Delta V_{SP} \approx 9.0\%$ left, $\pm$ 1.2%

$\Delta t_r \approx +64.2\%, \pm 17.5\%$

$^{+}t_r = t_{90\%} - t_{10\%}$

**Setting 1-3**

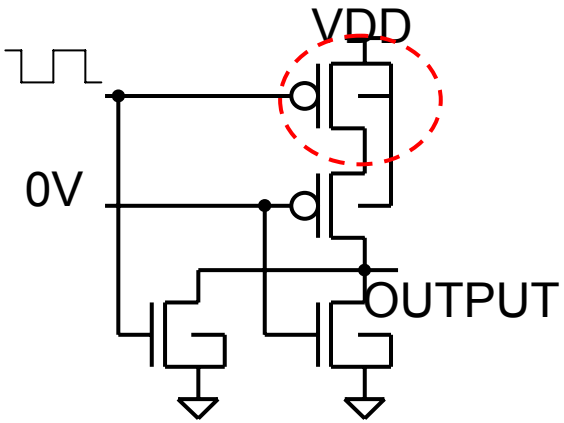


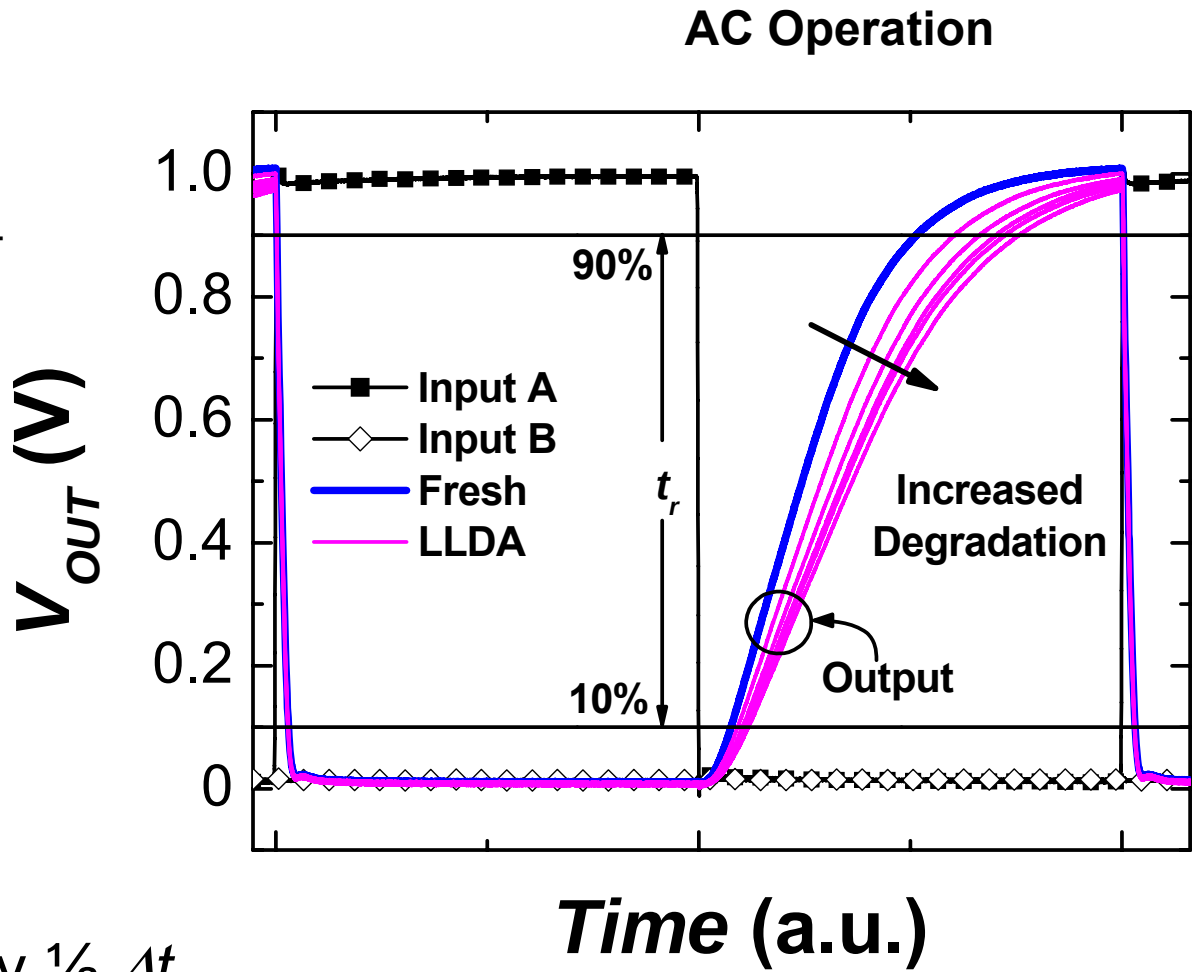

- Significant reduction in NAND circuit performance

[†]R. J. Baker, "CMOS: Circuit design, layout, and simulation," 2 ed: IEEE Press Wiley-Interscience, pp 317-318, 2005.

# 2nm NOR Gate V-t Response

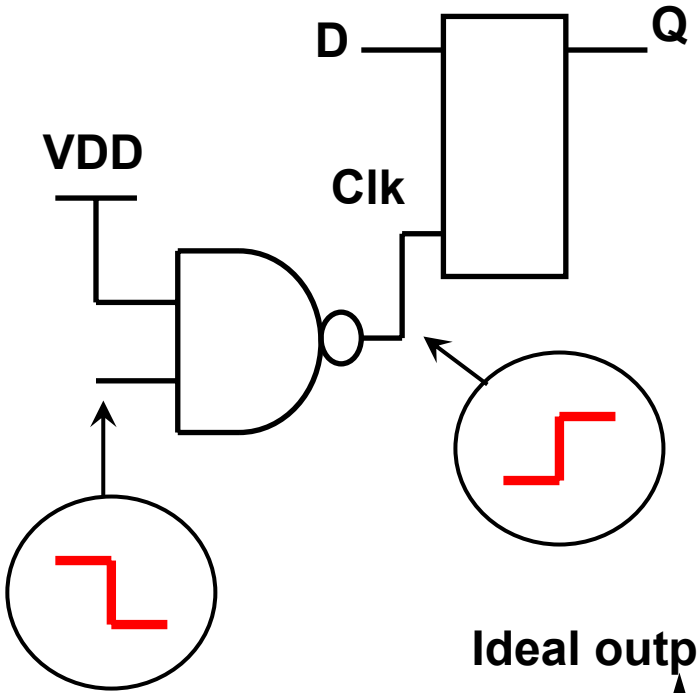



$\Delta t_r \approx +31\% \pm 6\%$



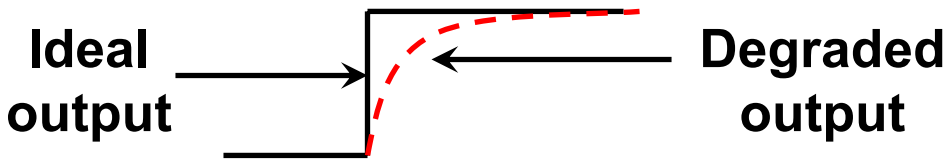

- Approximately ½ $\Delta t_{r,NAND}$
- Significant reduction in NOR circuit performance

# NAND Gate - Potential Circuit Failure



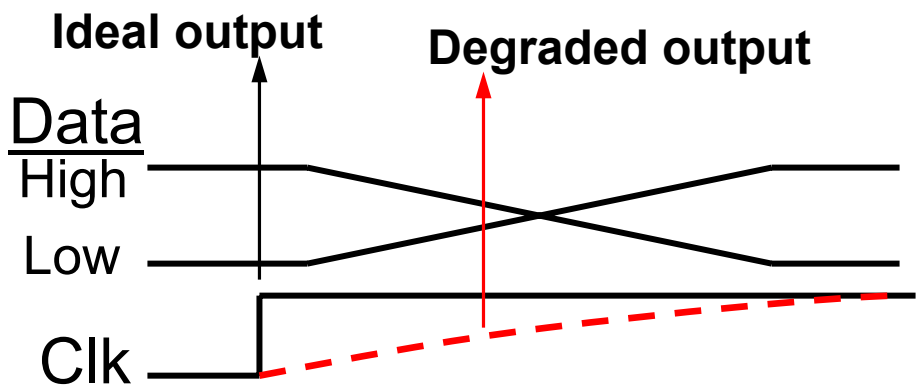

**Want: $t_{delay} < t_{setup}$**

**If $t_{delay}$ ↑ then output becomes:**




**Resulting problem:**

- **Does data get clocked?**
- **Too much delay → fail**



# SICBB - Conclusions

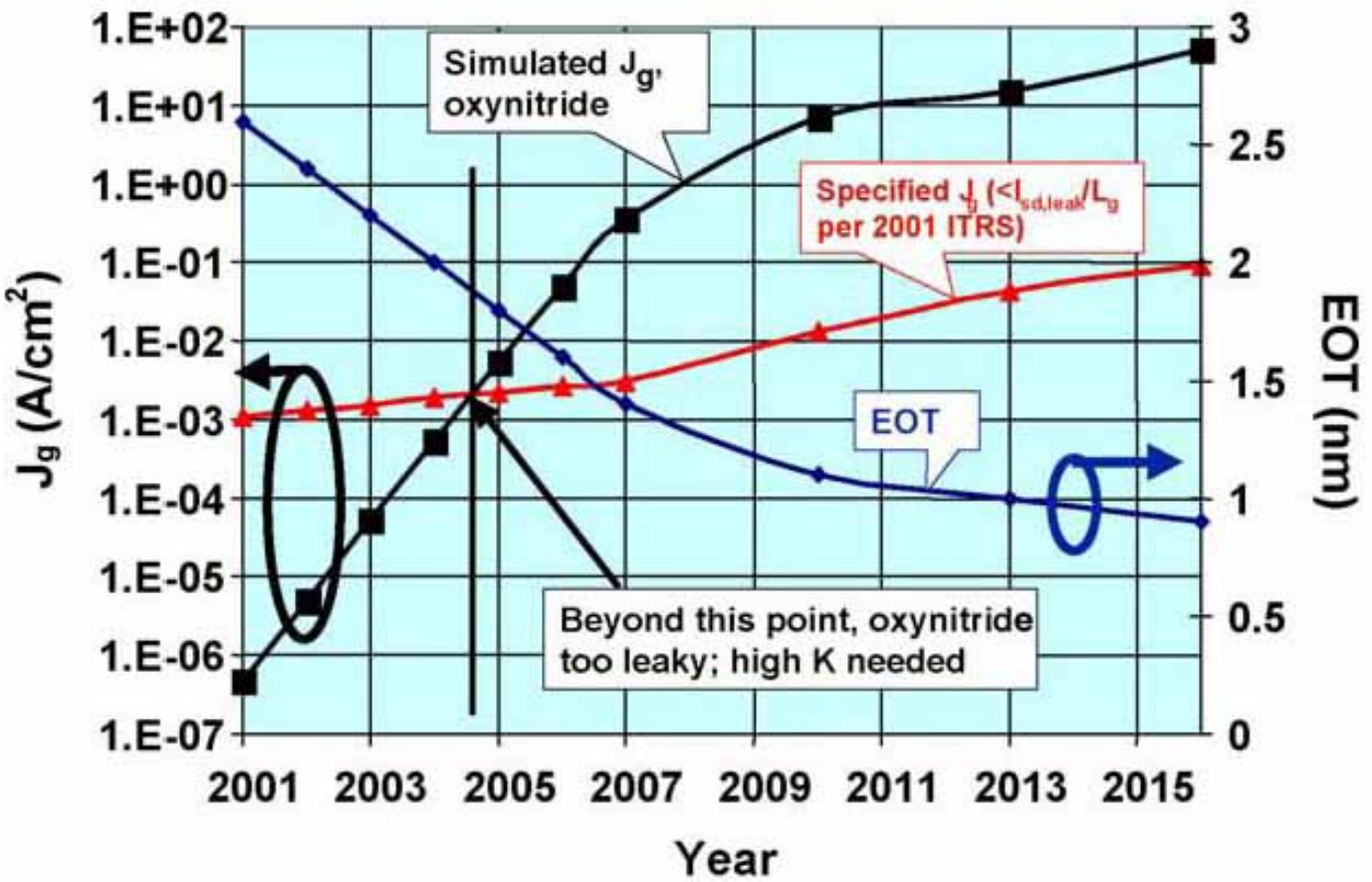
- Switch Matrix Technique – viable technique
  - Determine degradation in individual devices
  - Ability to connect device degradation to circuit degradation
- Gate Oxides: 2.0 nm more susceptible than 3.2 nm to EM-radiation-like degradation
  - SICBB failure may result at a fairly low level degradation
- VTC measurements may show negligible inverter degradation
  - Suggests Oxide degradation effects in SICBBs <u>are not</u> a reliability issue
- Decrease in logic gate performance, particularly in time domain, directly related to:

$$\Delta I_{DRIVE} \longrightarrow I_{DRIVE} \propto \frac{1}{R_{CH}} \longrightarrow \Delta t_r \propto \Delta R_{CH}$$

- Observed degradation in $\Delta t_r$ of the NOR gate is about half of that observed in NAND gates

# High k Dielectrics to Replace $SiO_2$

- Motivation



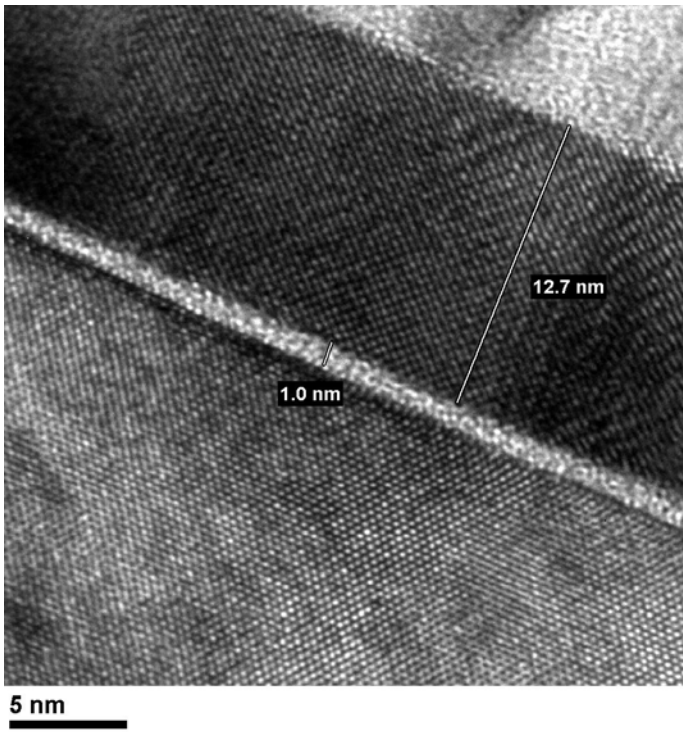

Leading high k candidate: $HfO_2$

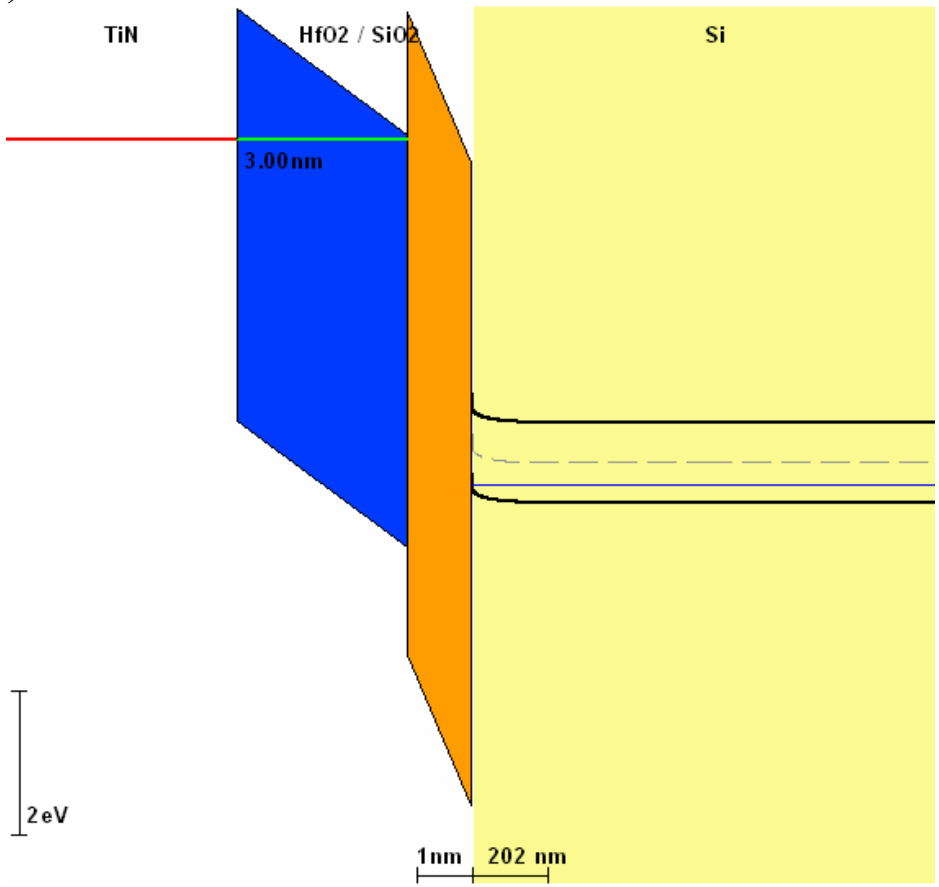
Dielectric Constant: ~25

M. Houssa *et al.*, Materials Science and Engineering R, vol. 51, pp. 37-85, 2006.

# High k Dielectrics – $HfO_2$

- Many Issues with $HfO_2$:
  - Prompted by $SiO_x$ interfacial layer (IL)
  - Larger number of defects
  - Reliability Assessment of IL needed

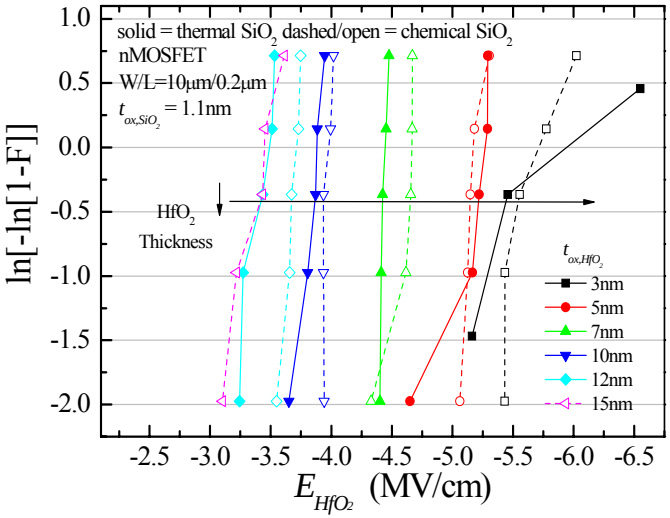


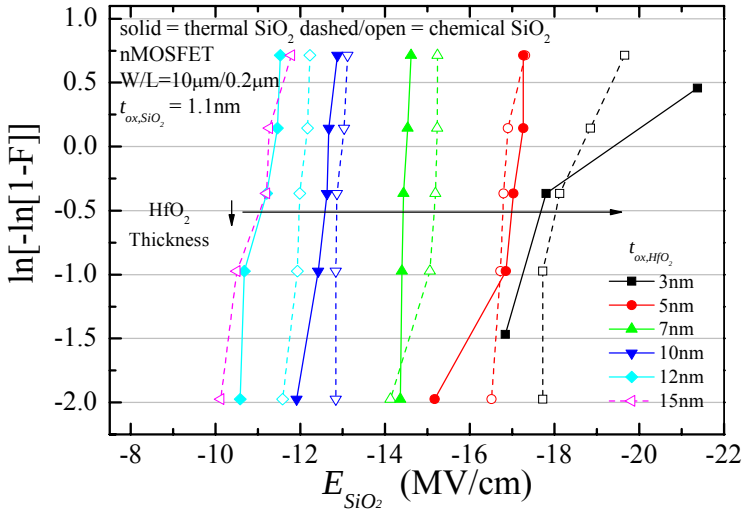



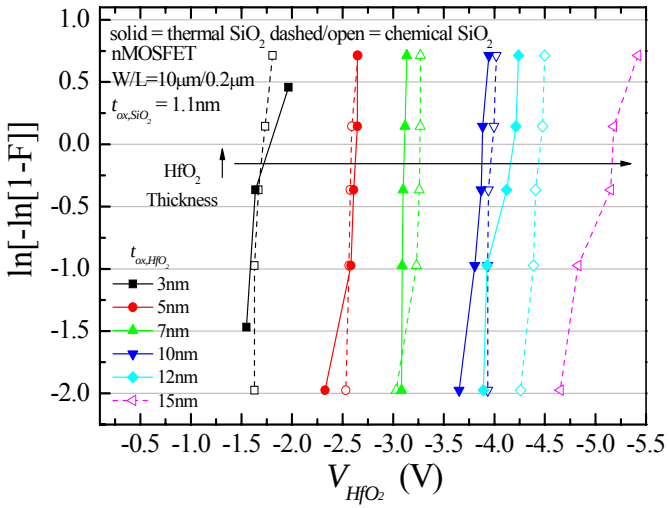

R. G. Southwick III and W. B. Knowlton, "Stacked dual oxide MOS energy band diagram visual representation program (IRW Student Paper)," *IEEE Transactions on Device and Materials Reliability*, accepted for publication, 2006.

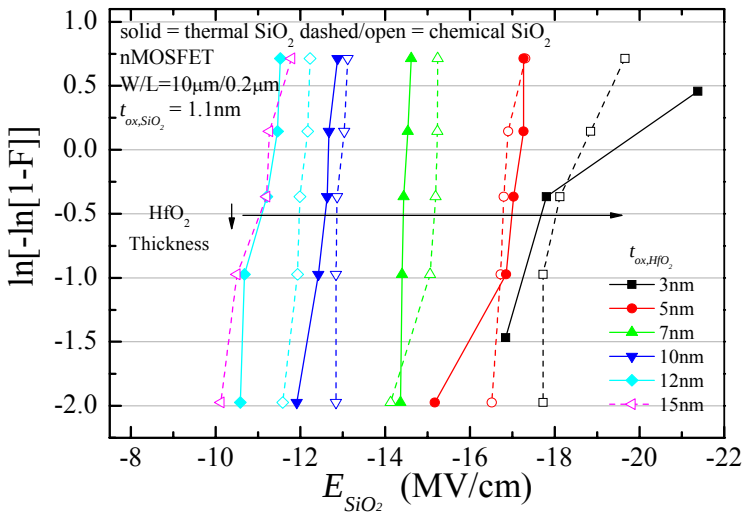
# $HfO_2$ – Preliminary RVS Reliability Testing

- Time-zero dielectric breakdown studies



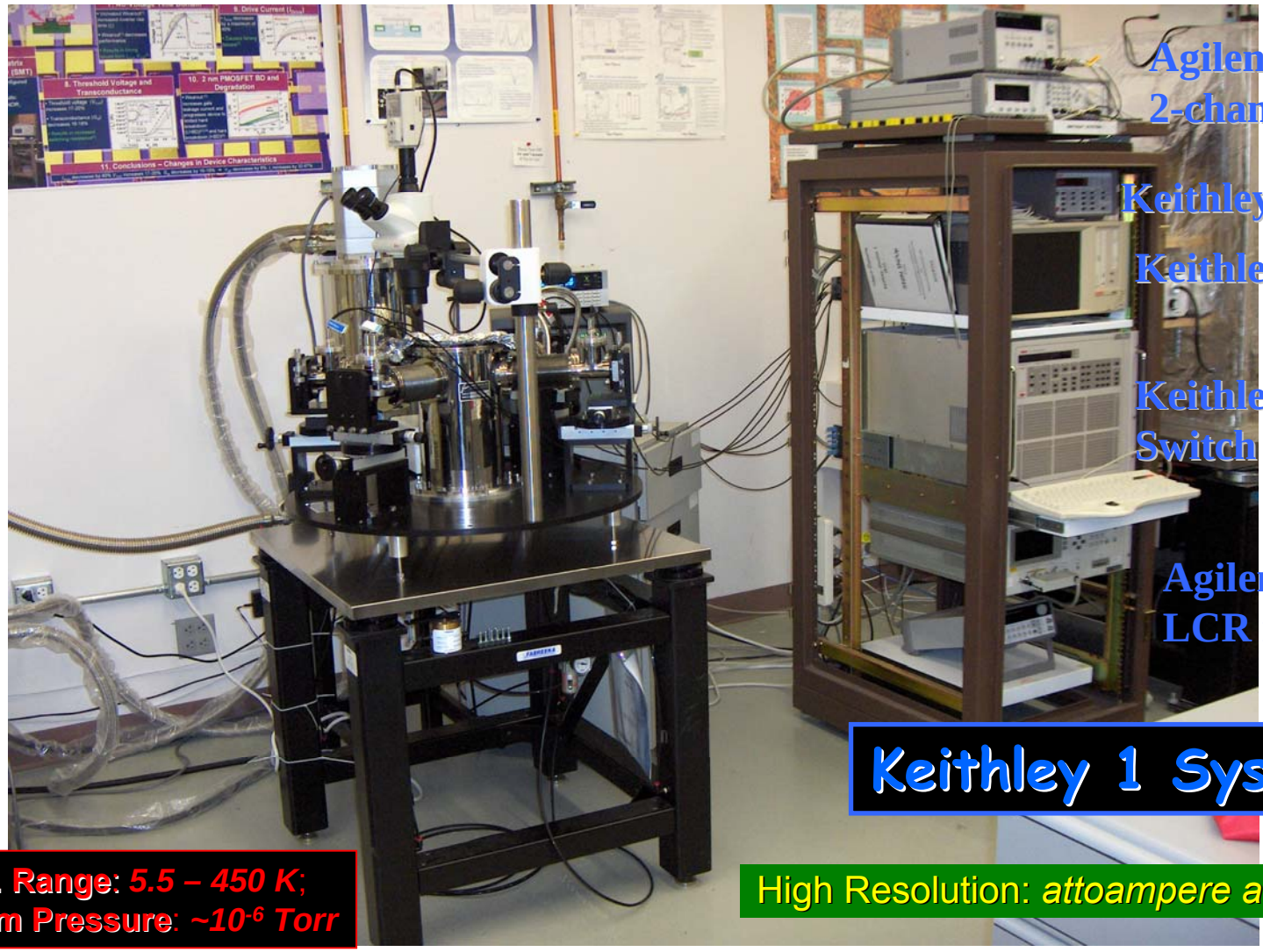



# **Future Work**: *Will use Variable Temperature Probestation*

- **Custom Design (3+ years in design & development)**

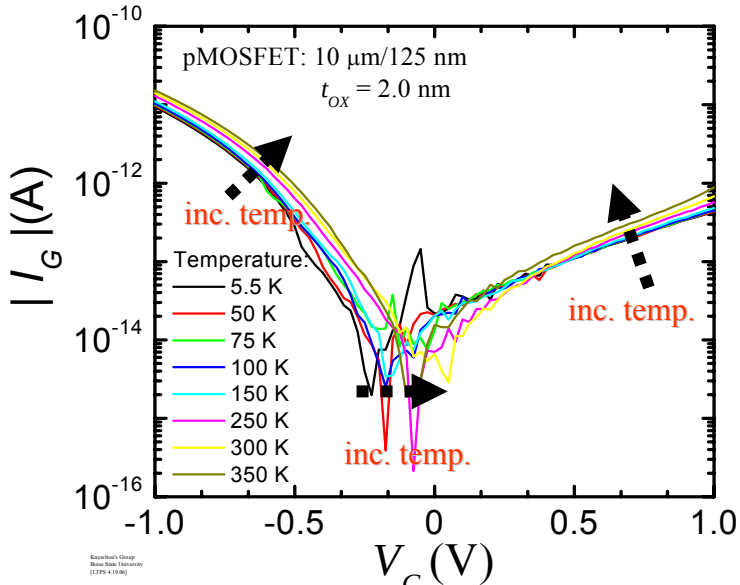


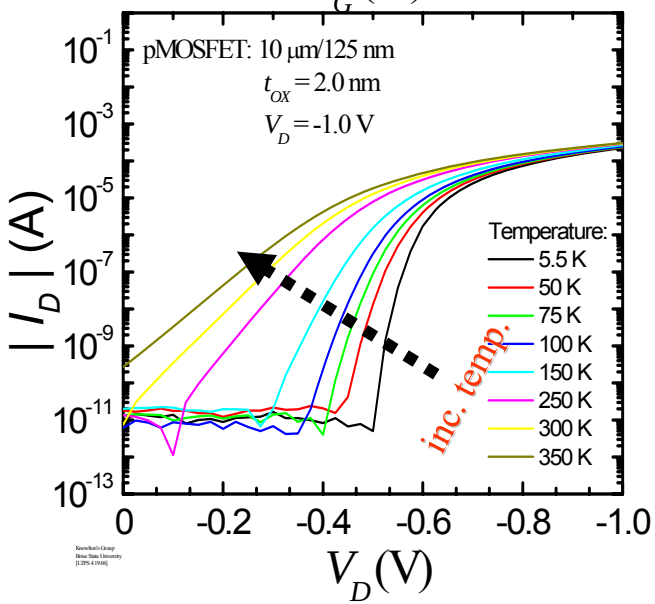

- Temp. Range: *5.5 – 450 K*;
- System Pressure: *~$10^{-6}$ Torr*

High Resolution: *attoampere and microvolt*

# Future Work: *Will use Variable Temperature Probestation*

- Cryogenic Temperature Studies
  - $SiO_2$ gate oxides
    - ✓ Device reliability
    - ✓ Circuit reliability
  - High dielectric constant reliability
- High temp measurements
  - Thermal stability
  - Reliability: thermal & voltage acceleration



# Thank you

- Questions?